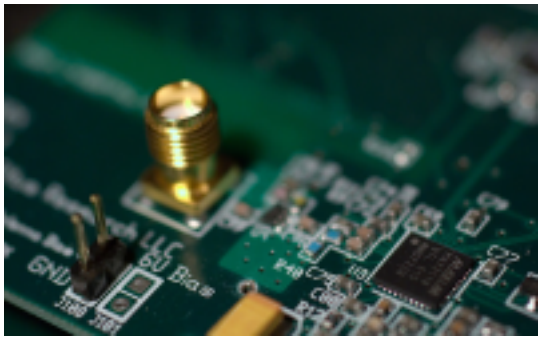
Chitlesh GOORAH

Design & Verification Club Bristol 2010



[Free Electronic Lab]

(formerly Fedora Electronic Lab)

An opensource Design and Simulation platform
for Micro-Electronics

A one-stop linux distribution for hardware design

Marketing means for opensource EDA developers (Networking)

From SPEC, Model, Frontend Design, Backend,
Development boards to embedded software.

Electronic Designers Problems

Approx. 6 month design development cycle

Tackling Design Complexity

Lower Power, Lower Cost and Smaller Space

Semiconductor Industry's neck squeezed in 2008

Management (digital/analog) IP Portfolio

OVERVIEW : FEL'S SOLUTIONS TO THE DESIGN CENTER

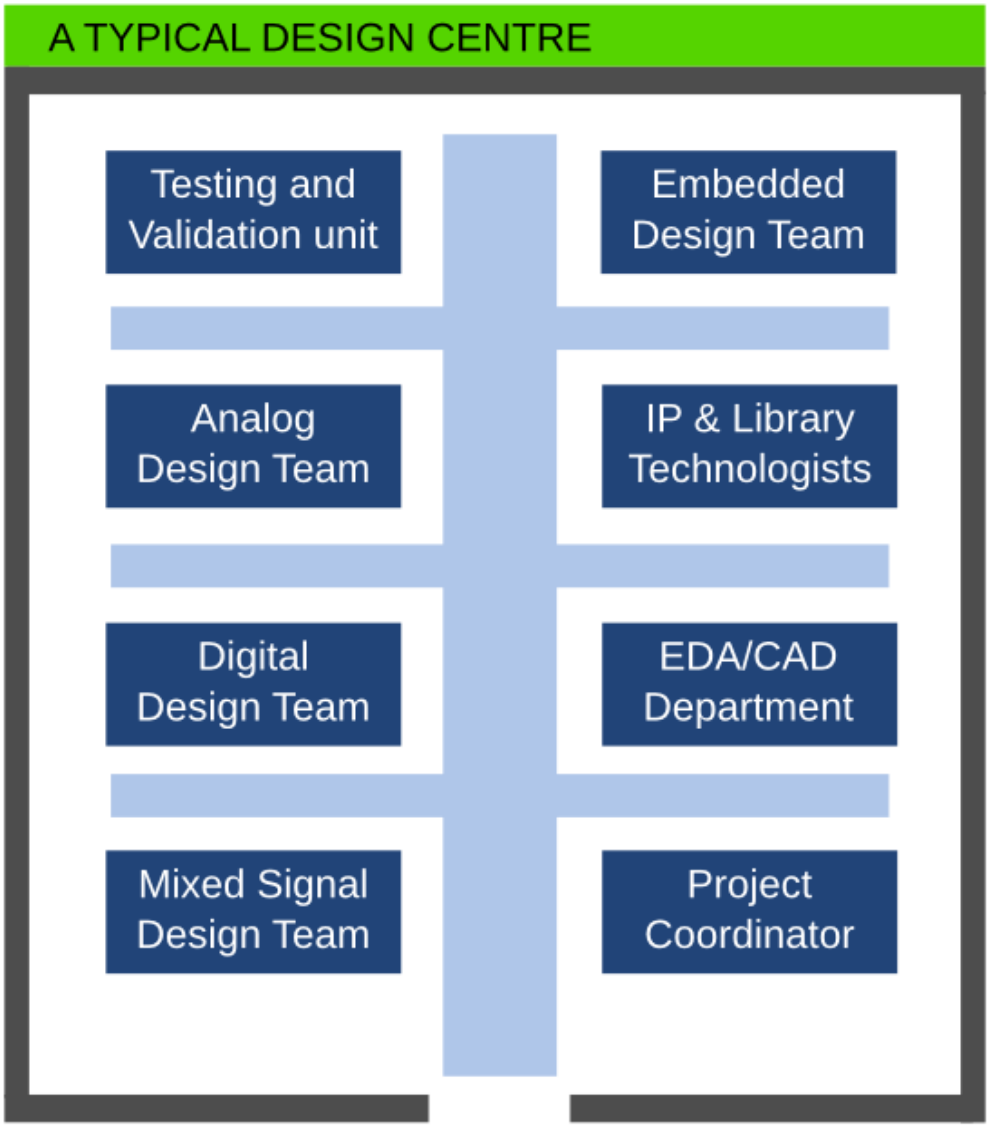
Providing EDA solutions for the real world requires a clear overview on the targetted users.

Free Electronic Lab strives to fulfill all the needs of each stage of the design flow .

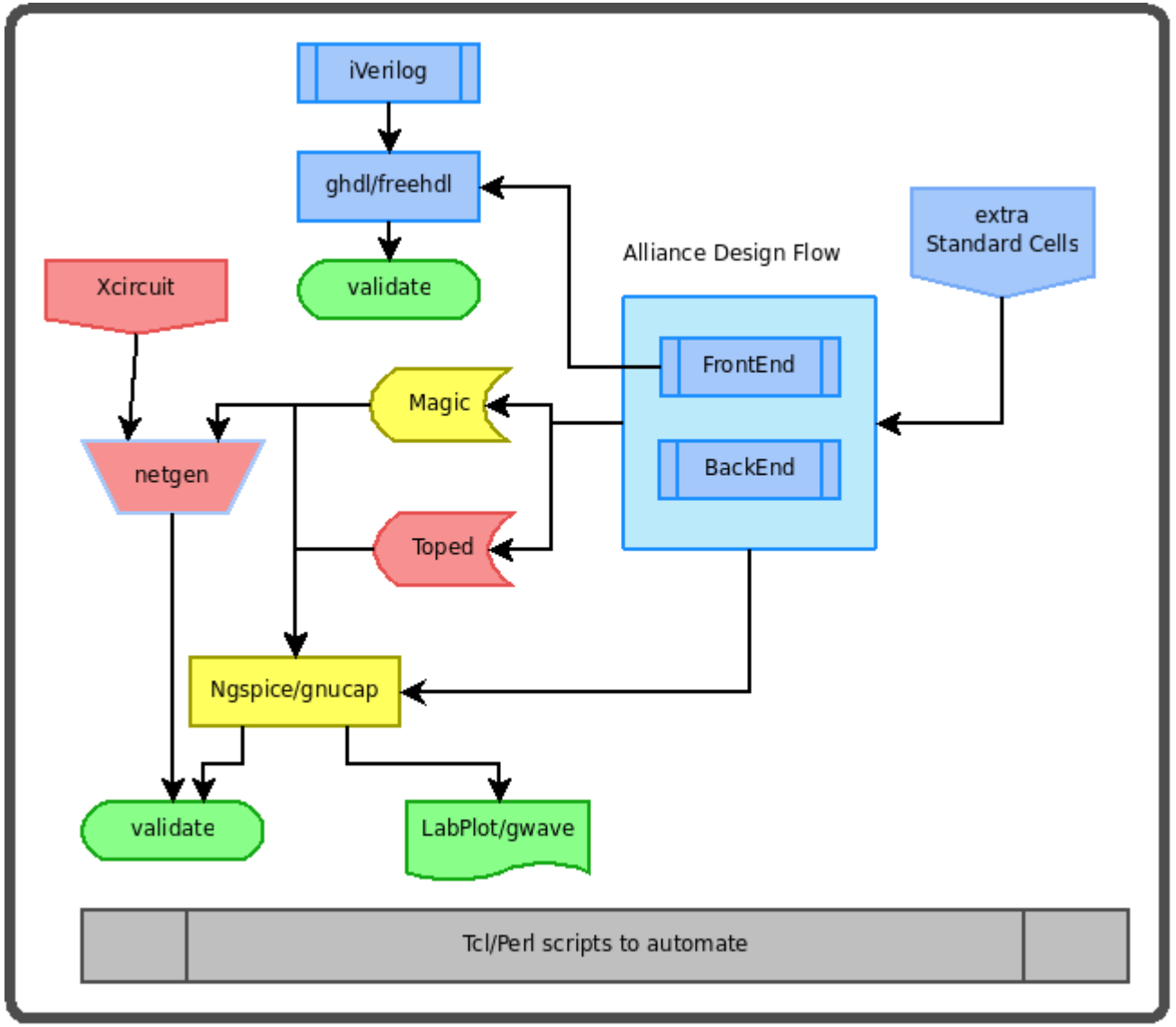
Free Electronic Lab

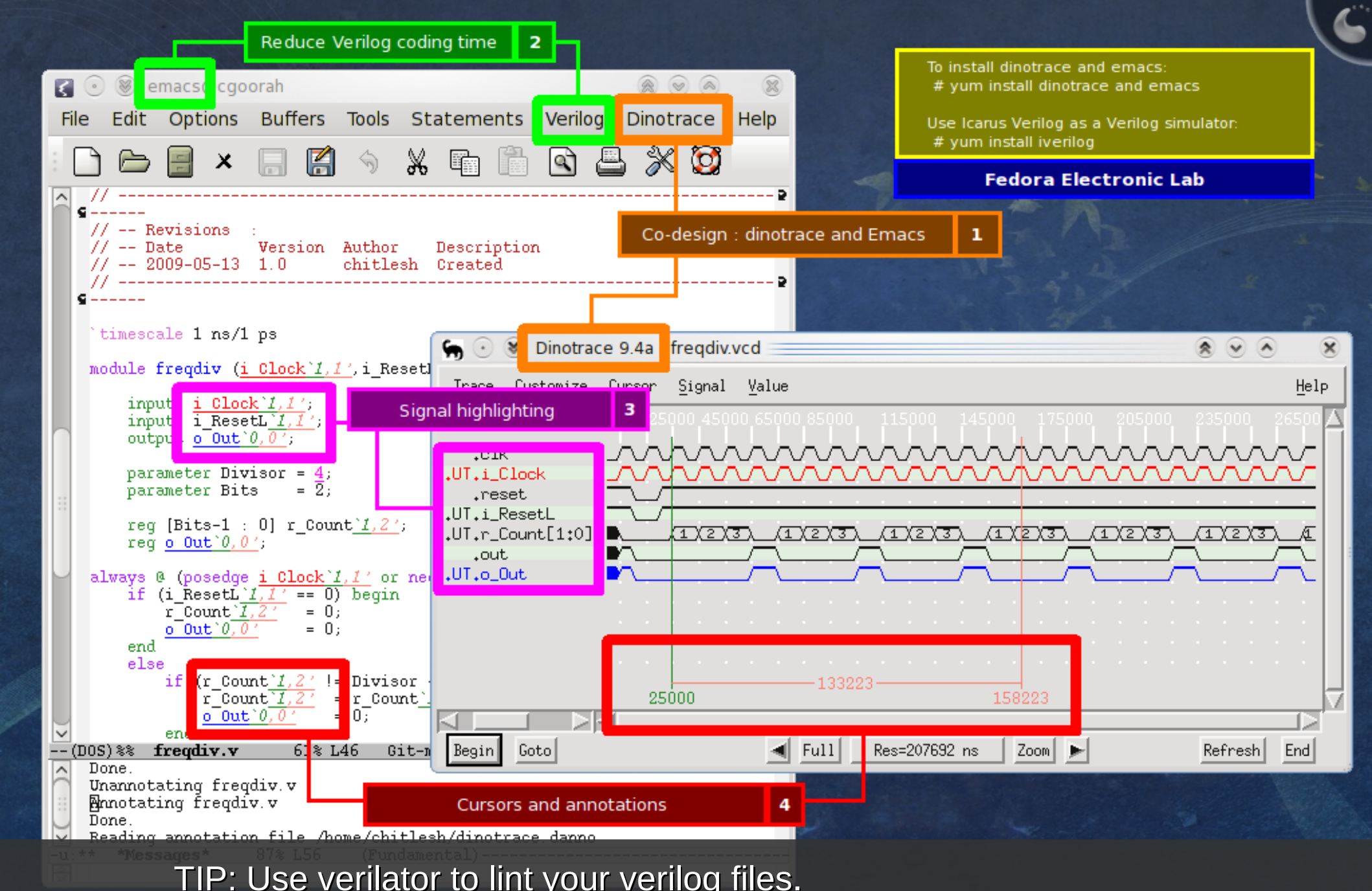
Free Electronic Lab improves hardware design experience with opensource software.

http://chitlesh.fedorapeople.org/FEL



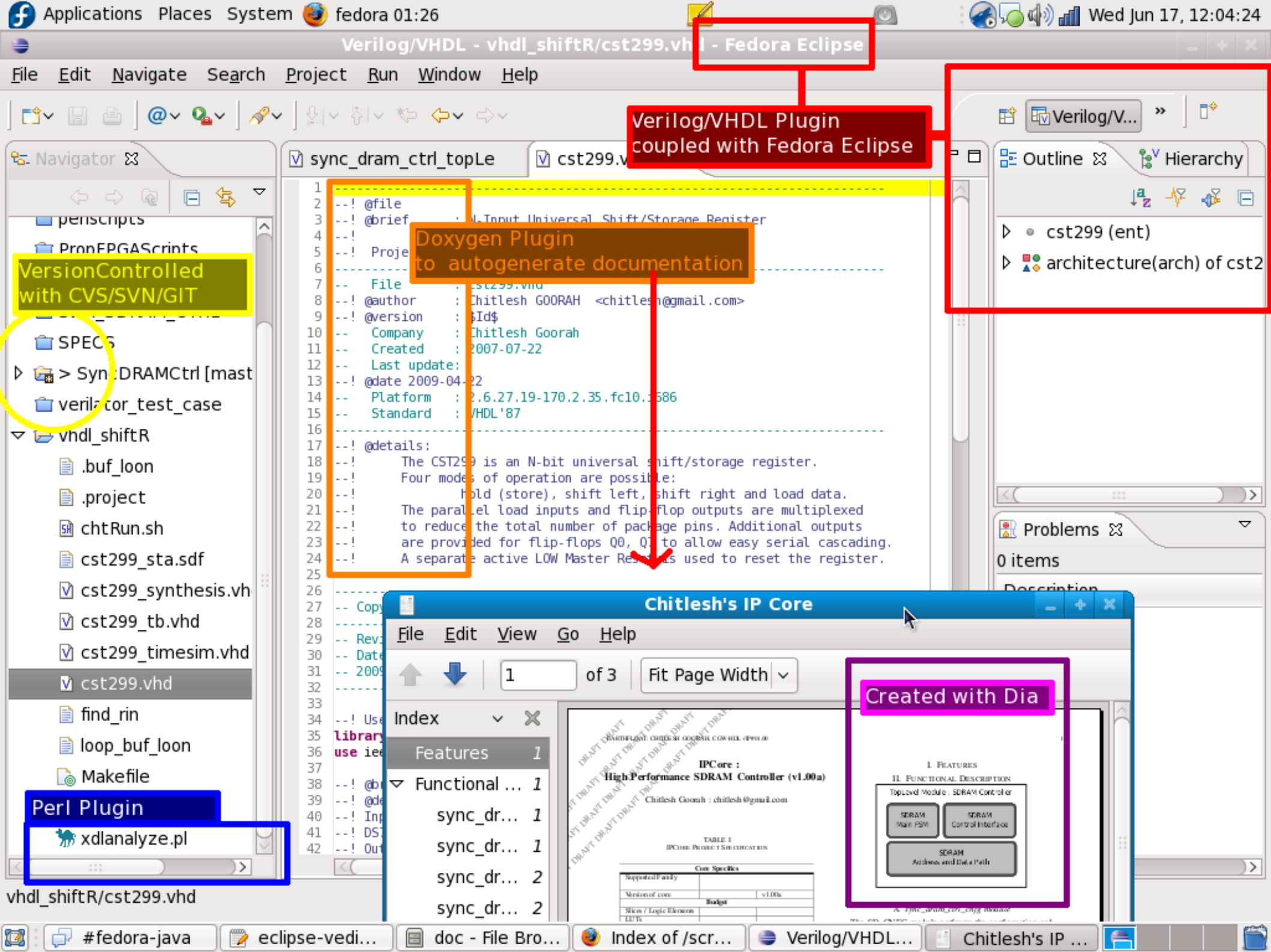
A basic Design Flow

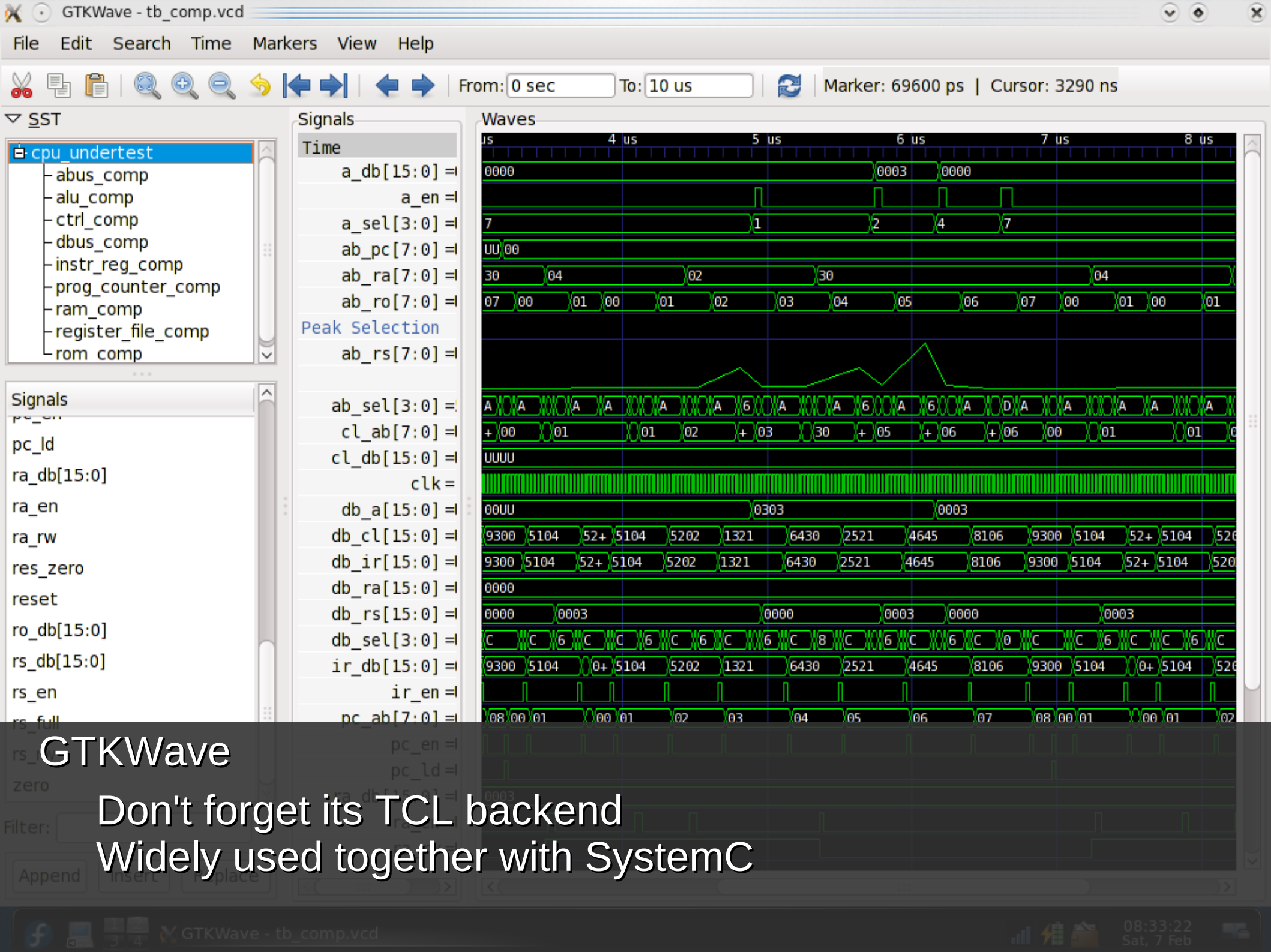




TIP: Use verilator to lint your verilog files.

Most of the Veripool tools are available under FEL.
They are in sync with Wilson Snyder's releases.


Applications Places System fedora 01:26
Wed Jun 17, 12:04:24
Verilog/VHDL - vhdl_shiftR/cst299.vhd - Fedora Eclipse
File Edit Navigate Search Project Run Window Help
Verilog/VHDL Plugin coupled with Fedora Eclipse
Navigator
VersionControlled with CVS/SVN/GIT
SPECS
vhdl_shiftR
.buf_loon
.project
chtRun.sh
cst299_sta.sdf
cst299_synthesis.vh
cst299_tb.vhd
cst299_timesim.vhd
cst299.vhd
find_rin
loop_buf_loon
Makefile
Perl Plugin
xdlanalyze.pl
vhdl_shiftR/cst299.vhd
Doxygen Plugin to autogenerate documentation
sync_dram_ctrl_topLe
cst299.v
--! @file
--! @author : Chitlesh GOORAH <chitlesh@gmail.com>
-- Company : Chitlesh Goorah
-- Created : 2007-07-22
--! @date 2009-04-22
-- Standard : VHDL'87
--! @details:
--! The CST299 is an N-bit universal shift/storage register.
--! Four modes of operation are possible:
--! The parallel load inputs and flip-flop outputs are multiplexed
--! to reduce the total number of package pins. Additional outputs
--! are provided for flip-flops Q0, Q7 to allow easy serial cascading.
--! A separate active LOW Master Reset is used to reset the register.
Outline
Hierarchy
cst299 (ent)
architecture(arch) of cst2
Problems
0 items
Chitlesh's IP Core
File Edit View Go Help
1 of 3
Fit Page Width
Index
Features 1
Functional ... 1
sync_dr... 1
sync_dr... 1
sync_dr... 2
sync_dr... 2
IPCore :
High-Performance SDRAM Controller (v1.00a)
Chitlesh Goorah : chitlesh@gmail.com
Created with Dia
#fedora-java
eclipse-vedi...
doc - File Bro...
Index of /scr...
Verilog/VHDL...
Chitlesh's IP ...


GTKWave - tb_comp.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 10 us
Marker: 69600 ps | Cursor: 3290 ns
SST
cpu_undertest
abus_comp
alu_comp
ctrl_comp
dbus_comp
instr_reg_comp
prog_counter_comp
ram_comp
register_file_comp
rom_comp
Signals
pc_ld
ra_db[15:0]
ra_en
ra_rw
res_zero
reset
ro_db[15:0]
rs_db[15:0]
rs_en
Signals
Time
a_db[15:0]
a_en
a_sel[3:0]
ab_pc[7:0]
ab_ra[7:0]
ab_ro[7:0]
Peak Selection
ab_rs[7:0]
ab_sel[3:0]
cl_ab[7:0]
cl_db[15:0]
clk
db_a[15:0]
db_cl[15:0]
db_ir[15:0]
db_ra[15:0]
db_rs[15:0]
db_sel[3:0]
ir_db[15:0]
ir_en
Waves
4 us
5 us
6 us
7 us
8 us
GTKWave
Don't forget its TCL backend
Widely used together with SystemC

Tools

Standard Cell libraries

xooi21 standard cell family

2-I/P exclusive NOR gate with 2-OR input

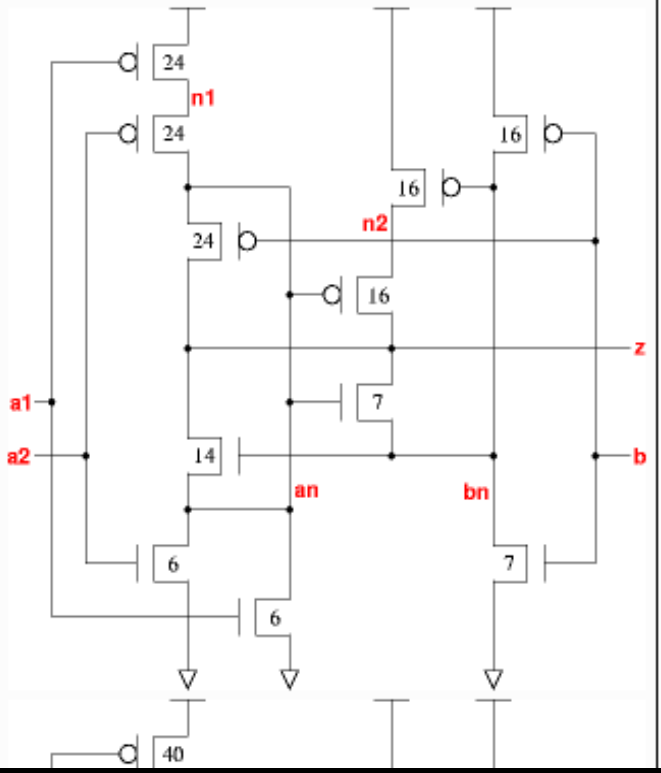
NEXT | PREV | UP

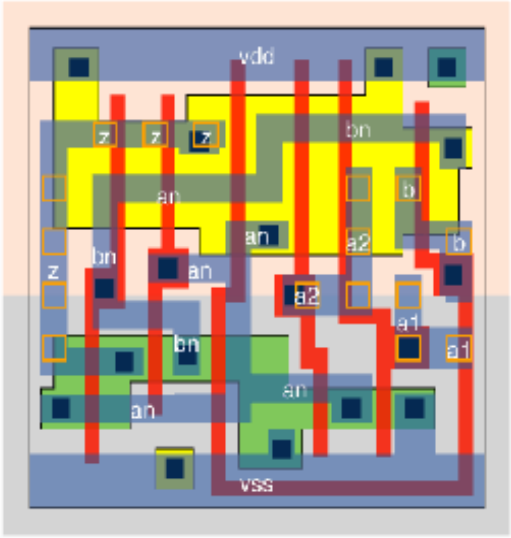
3 XNOR gates with OR gate input designed for minimum transistor count and hence smallest size. The OR gate is made by changing the inverter on the a input of a 2-XNOR gate into a 2-NOR gate. The Prop and Ramp delays below are the average of the inverting and non-inverting delays. The Synopsys Liberty format .LIB file has the correct delays for each case.

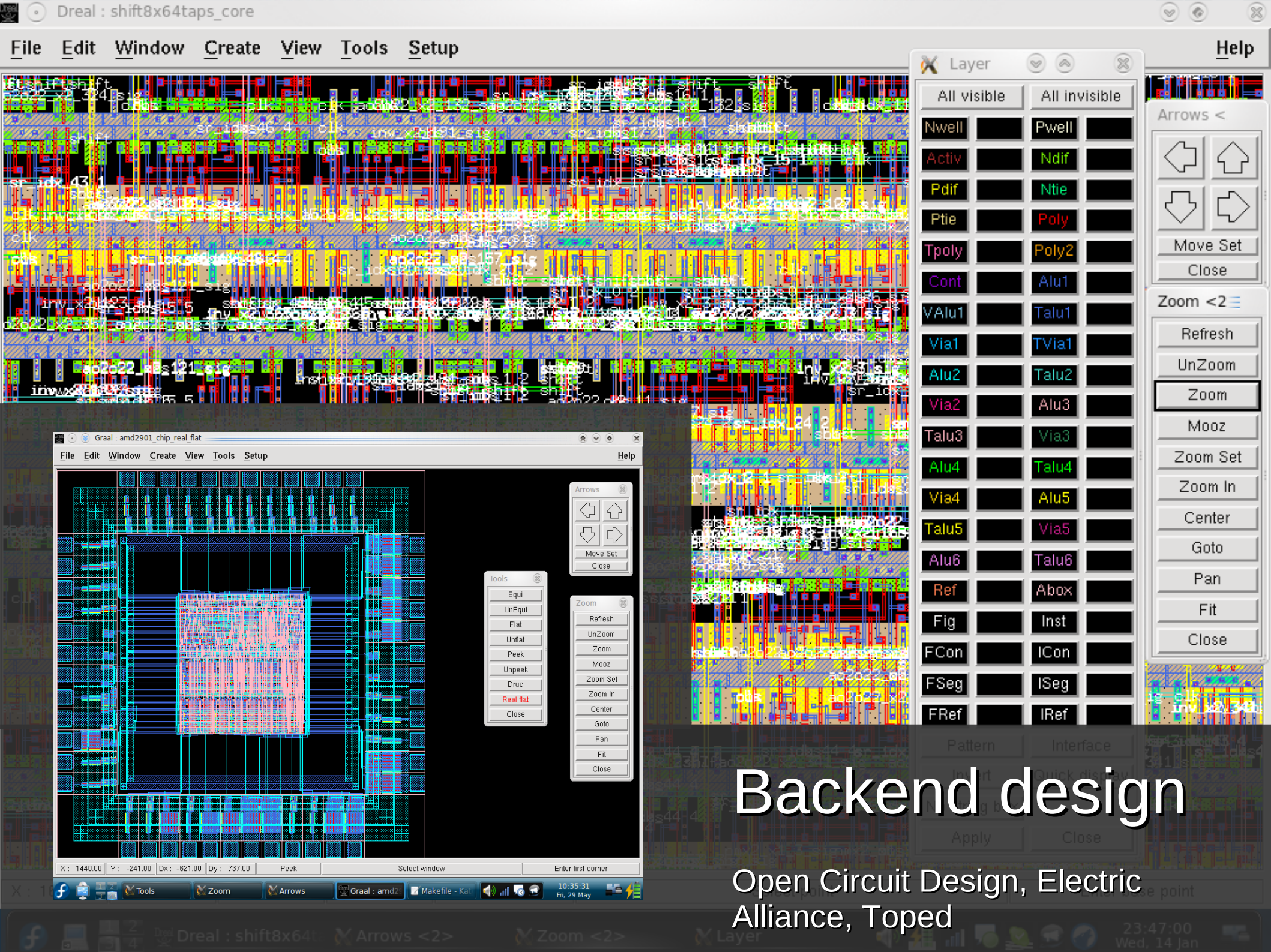
z:((a1+a2)^b)'	cell width			power		Generic 0.13um typical timing (ps & ps/fF), pin a2.				
				leakage	dynamic	tR=PropR+RampR×Load(fF), tF=PropF+RampF×Load(fF)				
vsclib013	gates	lambda	0.13um	nW	nW/MHz	PinCap	PropR	RampR	PropF	RampF
xooi21v0x05	3.0	72	3.96	0.87	19.7	3.7f	104	6.34	105	4.76
xooi21v0x1	4.0	96	5.28	1.52	29.6	6.0f	94	3.76	94	2.52
xooi21v0x2	6.7	160	8.80	2.73	56.8	11.2f	92	1.96	93	1.27

xooi21v0x05

		Effort	
		FO4	Log.
a1	/\	2.35	1.97
	-	3.22	
	_		
a2	/\	2.21	1.95
	-	3.13	
	_		
b	/\	2.41	3.06
	-	2.74	
	_		

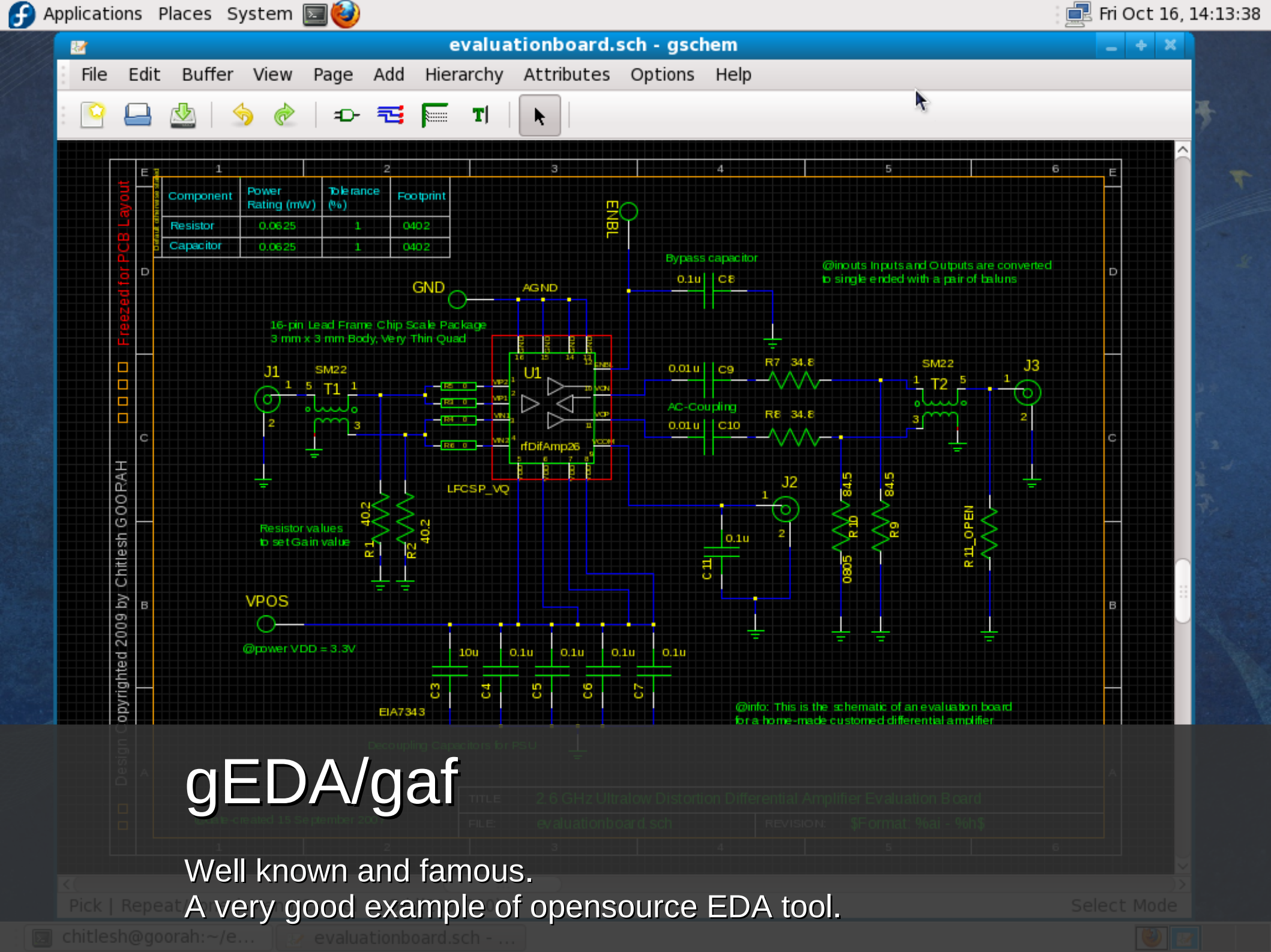






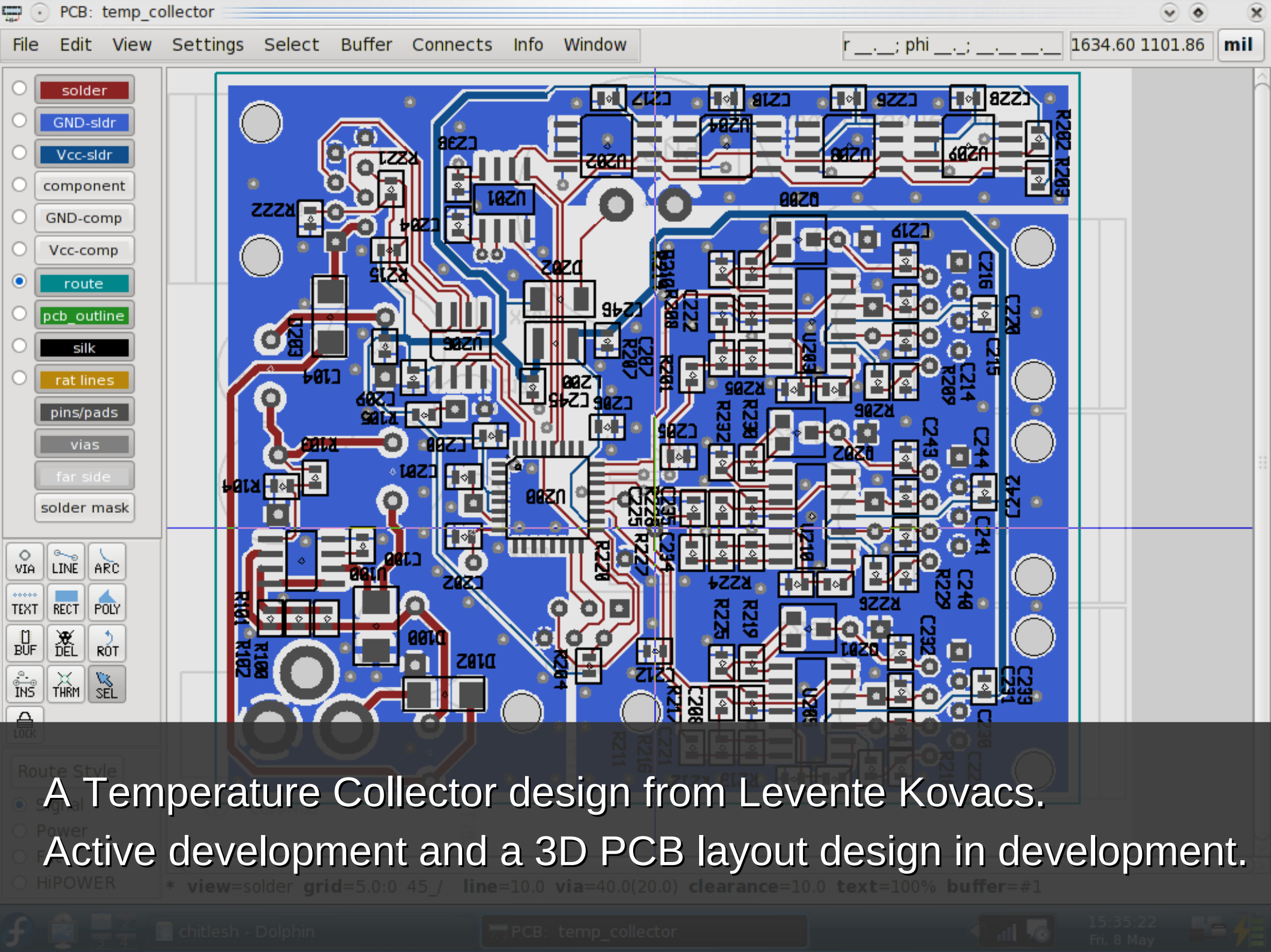
Backend design

Open Circuit Design, Electric
Alliance, Toped



gEDA/gaf

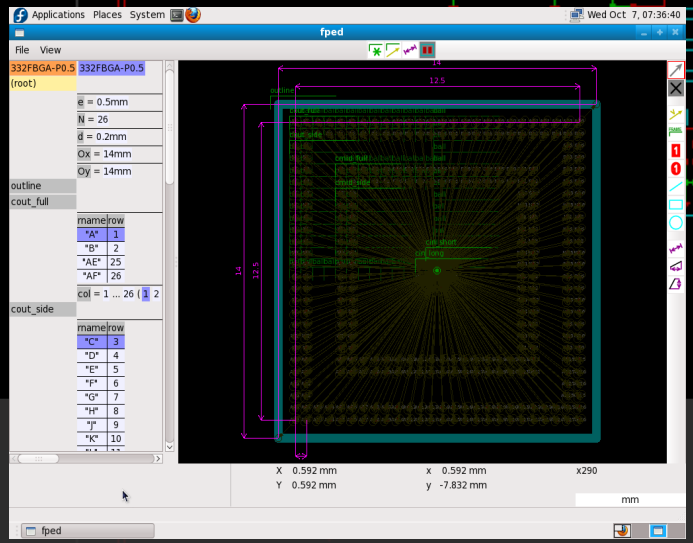
Well known and famous.
A very good example of opensource EDA tool.


PCB: temp_collector
File Edit View Settings Select Buffer Connects Info Window
1634.60 1101.86
mil
solder
GND-sldr
Vcc-sldr
component
GND-comp
Vcc-comp
route
pcb_outline
silk
rat lines
pins/pads
vias
far side
solder mask
VIA LINE ARC
TEXT RECT POLY
BUF DEL ROT
INS THRM SEL
LOCK
A Temperature Collector design from Levente Kovacs.
Active development and a 3D PCB layout design in development.

Applications Places System Wed Oct 7, 07:34:41

[gps.sch] Sheet /GPS/

File Edit View Place Preferences Help

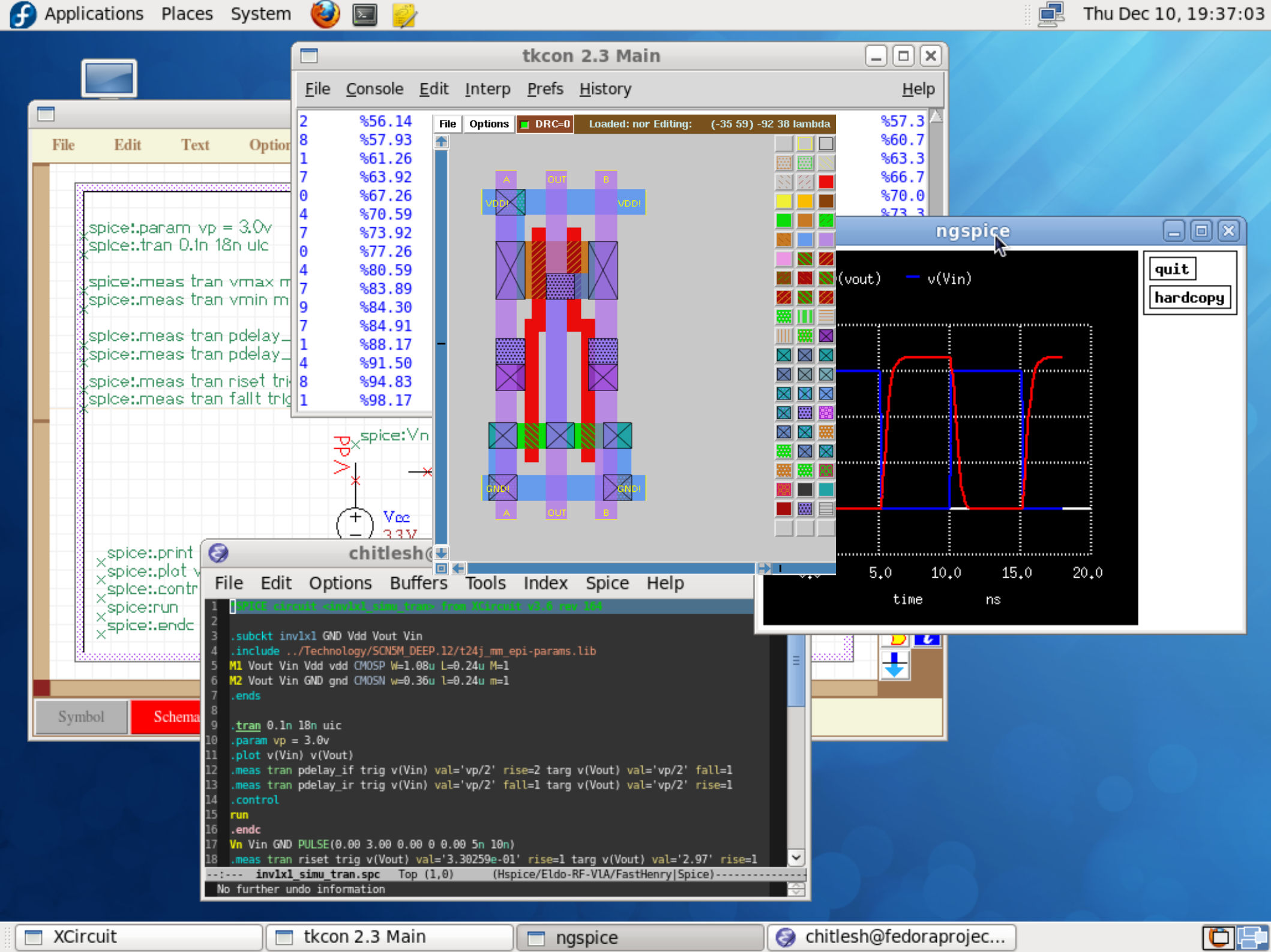


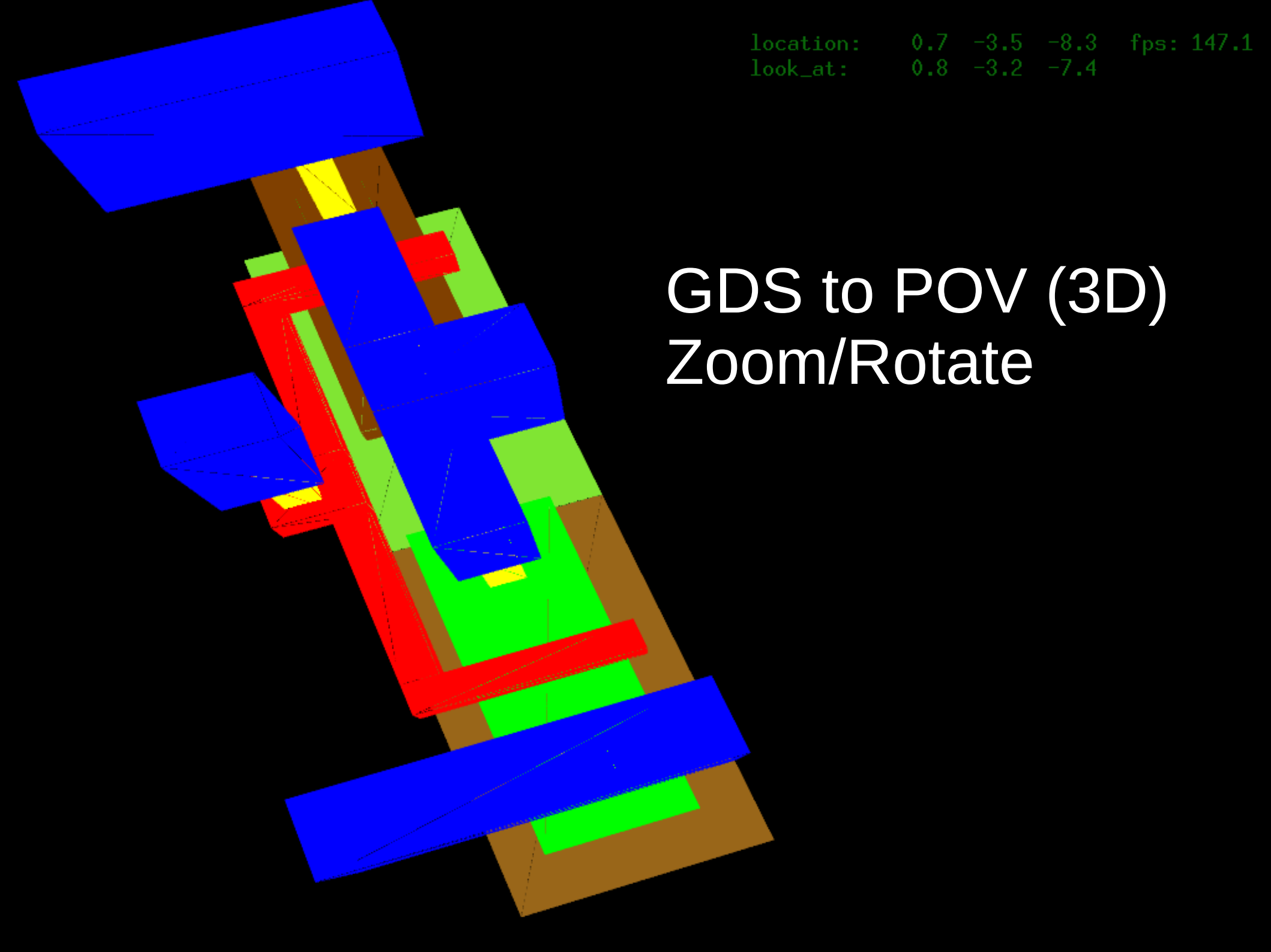
FEL's KICAD aligned with OpenMoko's needs

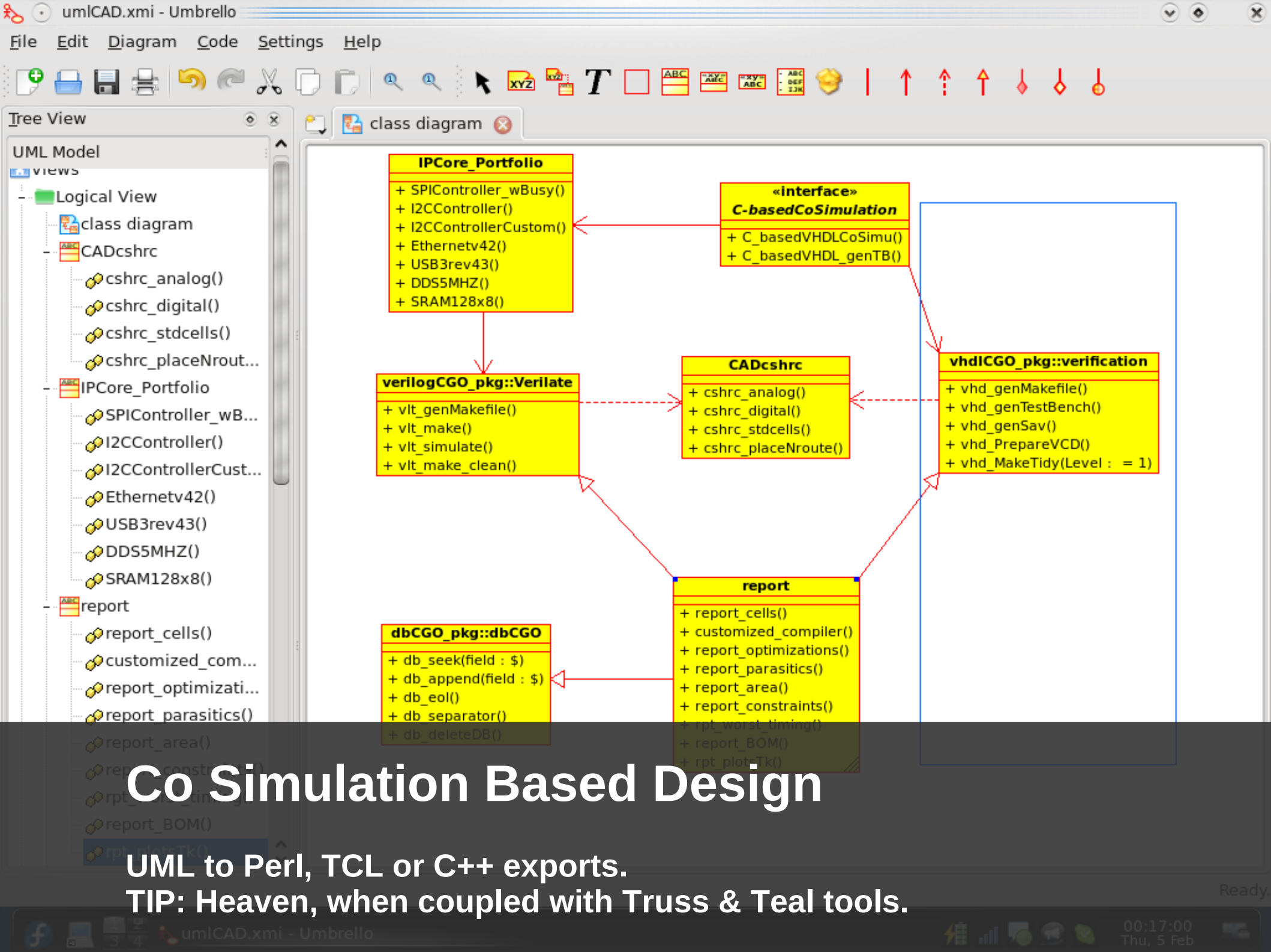
fped: OpenMoko's Footprint editor

Done Loading usb.sch Z 20.1 X 7.2500 Y 11.3500 x 1.4000 y 7.2170 Inch Push/Pop Hier

[gps.sch] Sheet /GPS/


Applications Places System
Thu Dec 10, 19:37:03
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
2 %56.14
8 %57.93
1 %61.26
7 %63.92
0 %67.26
4 %70.59
7 %73.92
0 %77.26
4 %80.59
7 %83.89
9 %84.30
7 %84.91
1 %88.17
4 %91.50
8 %94.83
1 %98.17
%57.3
%60.7
%63.3
%66.7
%70.0
File Options DRC=0 Loaded: nor Editing: (-35 59) -92 38 lambda
A OUT B
VDD! VDD!
GND! GND!
A OUT B
File Edit Text Option
spice:.param vp = 3.0v
spice:.tran 0.1n 18n uic
spice:.meas tran vmax m
spice:.meas tran vmin m
spice:.meas tran pdelay_
spice:.meas tran pdelay_
spice:.meas tran riset tri
spice:.meas tran fallt trig
spice:Vn
Vdd
Vcc
3.3V
spice:.print
spice:.plot v
spice:.contr
spice:run
spice:.endc
Symbol
Schema
ngspice
quit
hardcopy
(vout)
v(Vin)
5.0
10.0
15.0
20.0
time
ns
chitlesh@
File Edit Options Buffers Tools Index Spice Help
1 *SPICE circuit <invlxl_simu_tran> from XCircuit v3.6 rev 164
2
3 .subckt invlxl GND Vdd Vout Vin
4 .include ../Technology/SCN5M_DEEP.12/t24j_mm_epi-params.lib
5 M1 Vout Vin Vdd vdd CMOSP W=1.08u L=0.24u M=1
6 M2 Vout Vin GND gnd CMOSN w=0.36u l=0.24u m=1
7 .ends
8
9 .tran 0.1n 18n uic
10 .param vp = 3.0v
11 .plot v(Vin) v(Vout)
12 .meas tran pdelay_if trig v(Vin) val='vp/2' rise=2 targ v(Vout) val='vp/2' fall=1
13 .meas tran pdelay_ir trig v(Vin) val='vp/2' fall=1 targ v(Vout) val='vp/2' rise=1
14 .control
15 run
16 .endc
17 Vn Vin GND PULSE(0.00 3.00 0.00 0 0.00 5n 10n)
18 .meas tran riset trig v(Vout) val='3.30259e-01' rise=1 targ v(Vout) val='2.97' rise=1
--:--- invlxl_simu_tran.spc Top (1,0) (Hspice/Eldo-RF-VlA/FastHenry|Spice)
No further undo information
XCircuit
tkcon 2.3 Main
ngspice
chitlesh@fedoraprojec...


location: 0.7 -3.5 -8.3 fps: 147.1
look_at: 0.8 -3.2 -7.4
GDS to POV (3D)
Zoom/Rotate



Co Simulation Based Design

UML to Perl, TCL or C++ exports.
TIP: Heaven, when coupled with Truss & Teal tools.

OVERVIEW : A FREE HIGH END HARDWARE DESIGN PLATFORM

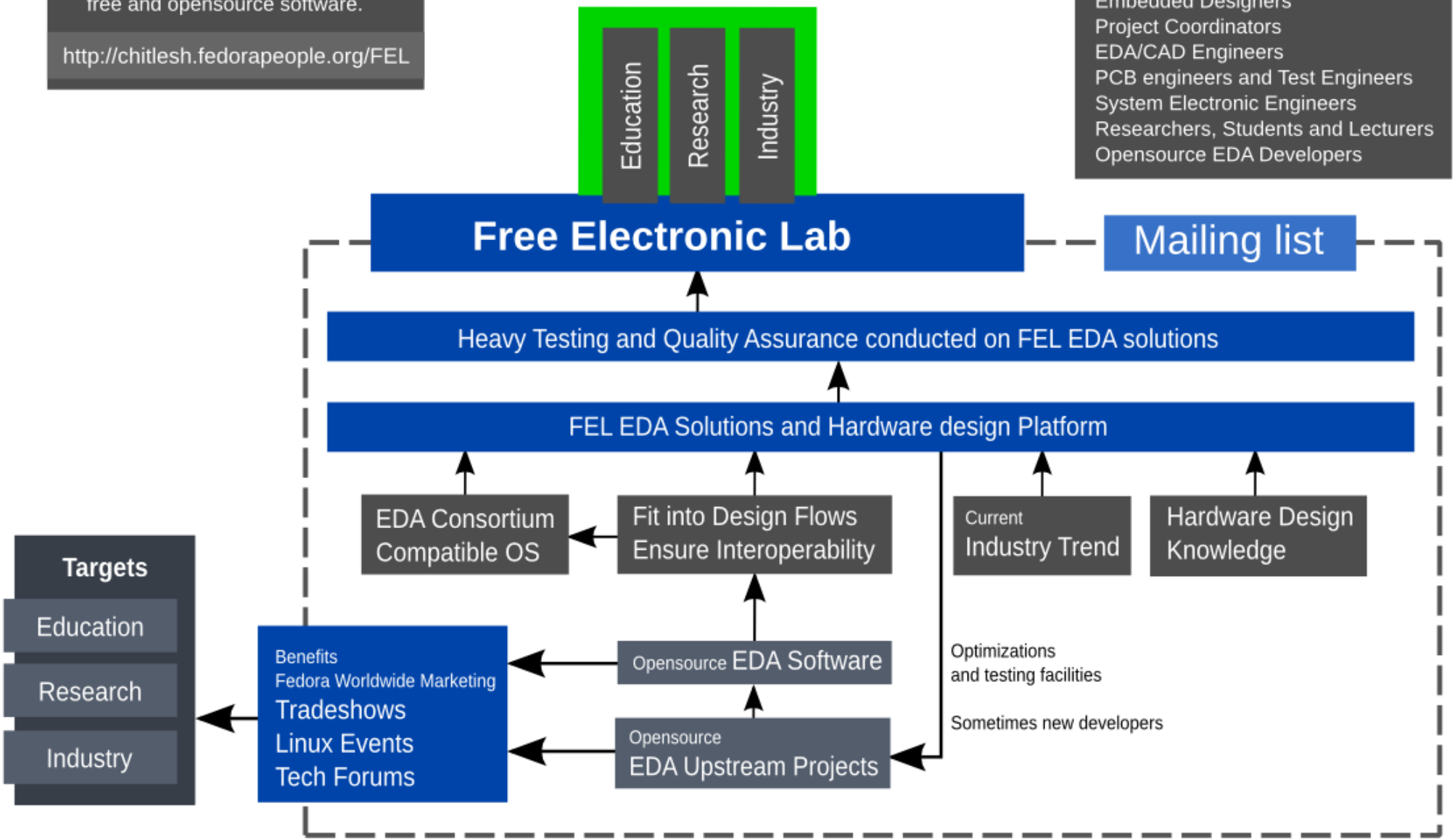
Free Electronic Lab

Free Electronic Lab improves hardware design experience with free and opensource software.

http://chitlesh.fedorapeople.org/FEL

Benefits

Analog/Digital/Mixed Designers
Verification solutions
Embedded Designers
Project Coordinators
EDA/CAD Engineers
PCB engineers and Test Engineers
System Electronic Engineers
Researchers, Students and Lecturers
Opensource EDA Developers



Simple Installation

Trial:

Fedora Electronic Lab LiveDVD

Production Environment:

On Fedora > 12 or upcoming RHEL / CentOS 6

```
# yum groupinstall 'Electronic Lab'
```

Who are using FEL ?

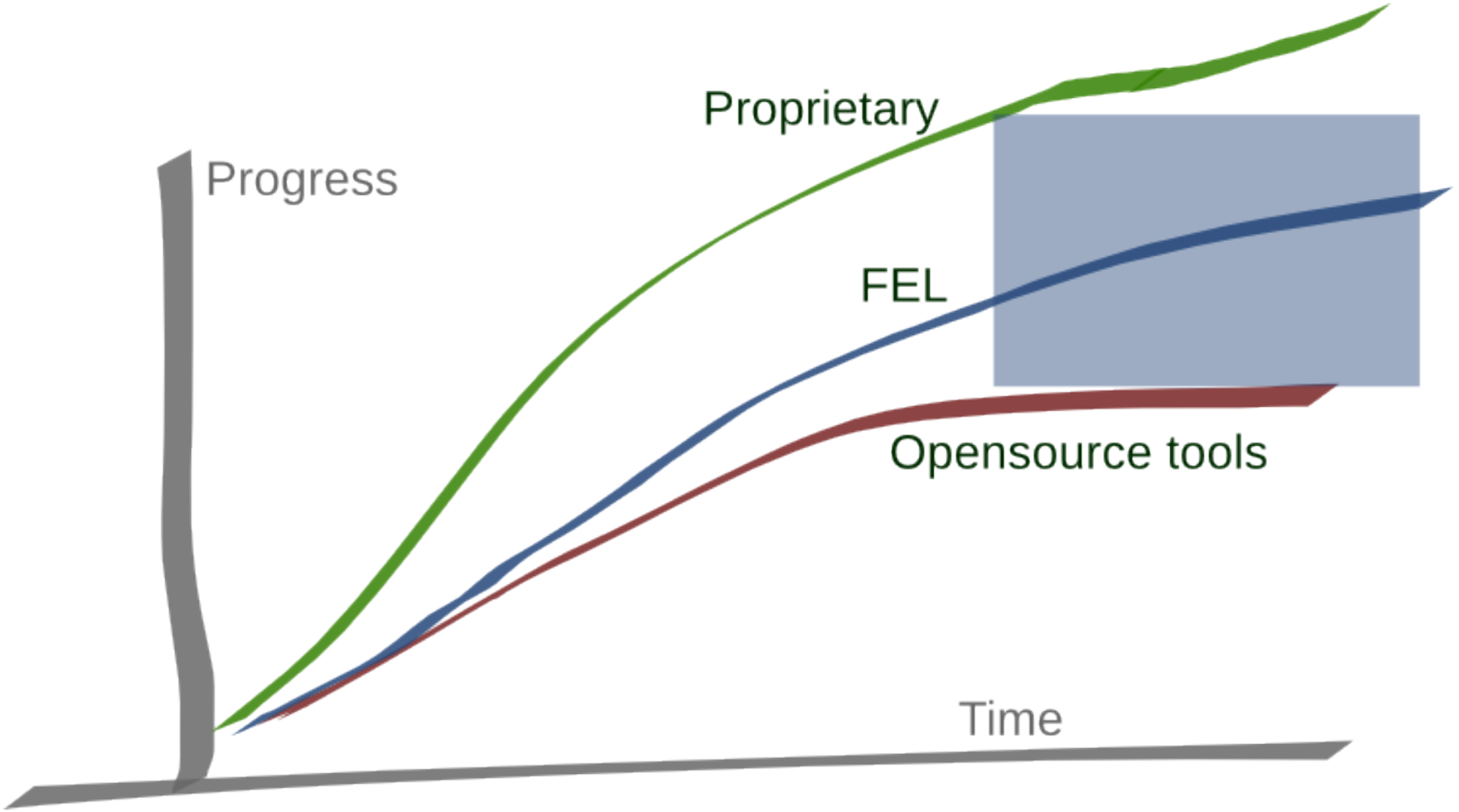
Universities around the world
- US, UK, France, India, Mexico, Brazil, Italy

Small companies & consulting companies

Linux For You magazine
Published twice (Jan 08, Jan 09)

Basic opensource EDA tools
Sun Microsystems, IBM, ST Microelectronics, Analog Devices, On Semi conductors

FEL User and Developer benefits



Free Electronic Lab 6.0 ?

- Satisfy User “ME”
- Strengthening the Backbone
- Ensuring Interchangeability
- FrontEnd design experience
- Port to the Entreprise Class OS
- Step into the opensource IP env

Questions & Answers

Thank you,

The Free Electronic Lab team

http://spins.fedoraproject.org/fel/
electronic-lab@lists.fedoraproject.org