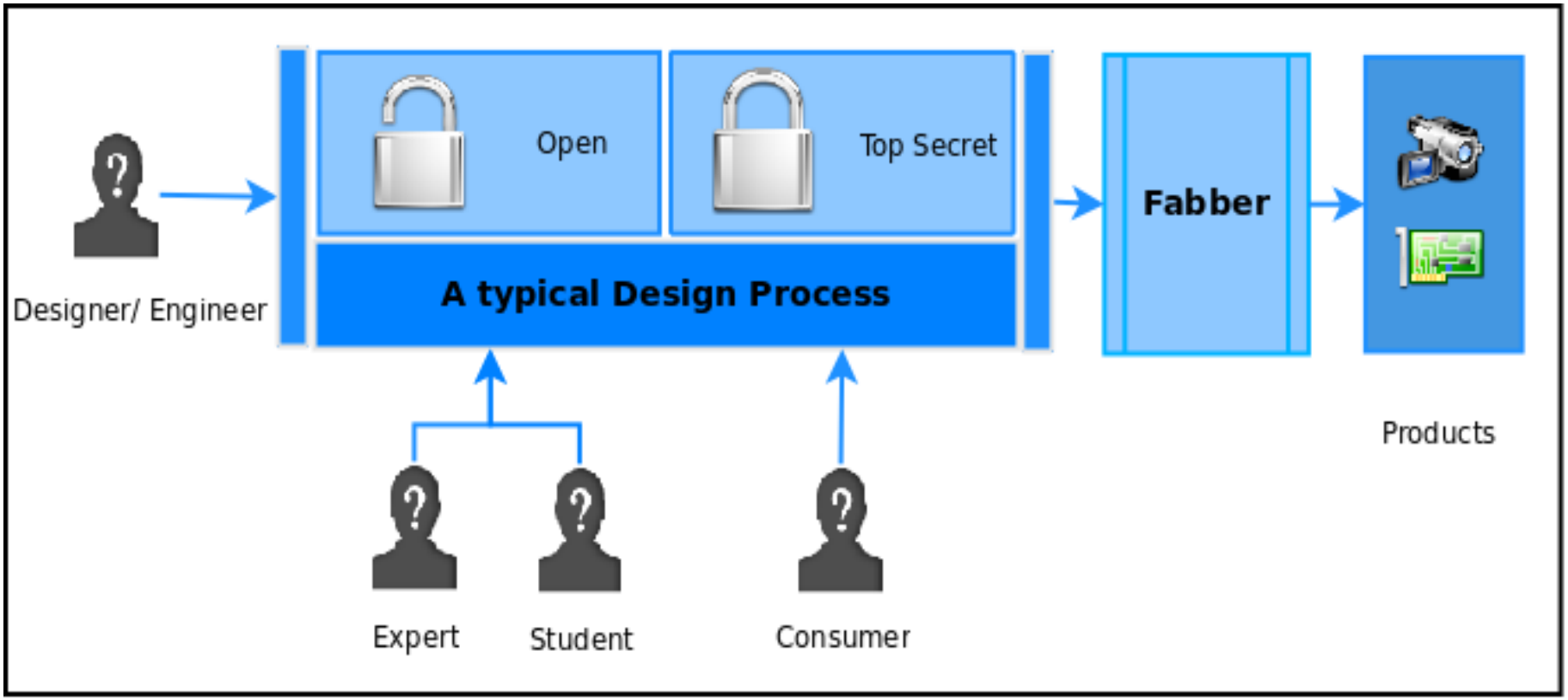
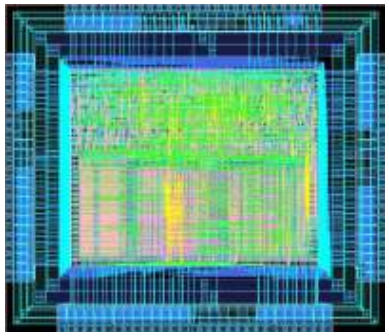
Fabless Semiconductor Business Model

Fedora Electronic Lab

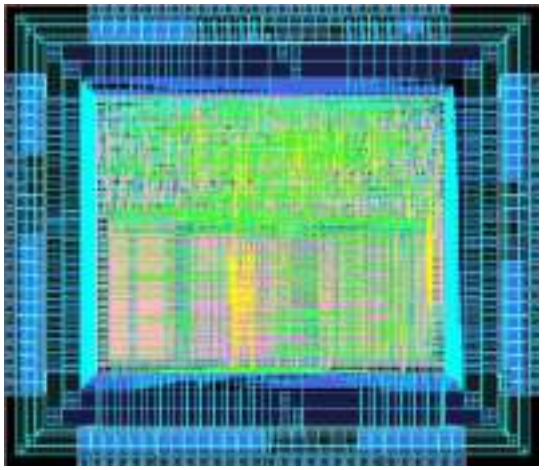
What is Fabless ?



Fabless v/s Business Solutions?



Designs



- Analog/Digital
- Circuit
- MicroControllers
- Embedded Systems

Design

Simulation

Verification

Business Solutions

- Solutions (methodologies, EDAs)
- Services (std cells, IPs, benchmarks)
- Technical Support (interoperability)
- Buy other small companies

Founder

- Manufacture
- CIF/GDSII
- Technical Support
- Packaging

Sale

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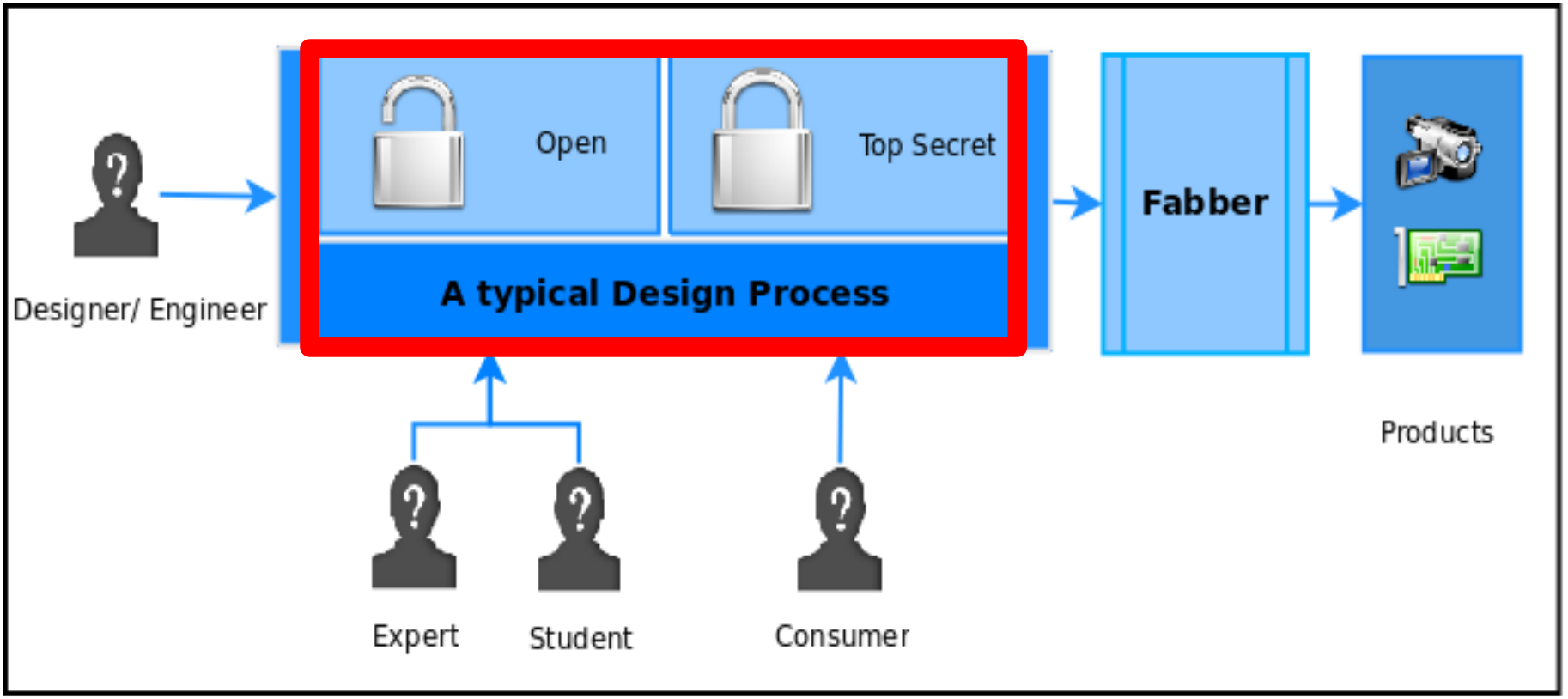

Understanding the needs

- High speeds simulation
- help designers stop burning time on non-critical busywork (mass deployments)
- Flows Move Toward Interoperability
- Achieving Accurate and Reliable Simulations

A unique open source Electronic Lab

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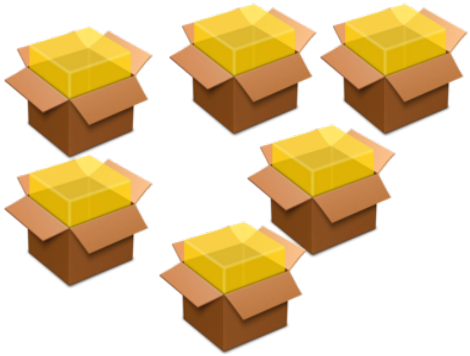
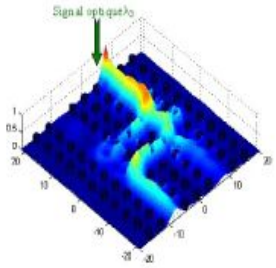


Patches / Packaging
Integration
Interoperability
Security Modules
Quality
Bugzilla, Revisor, spins

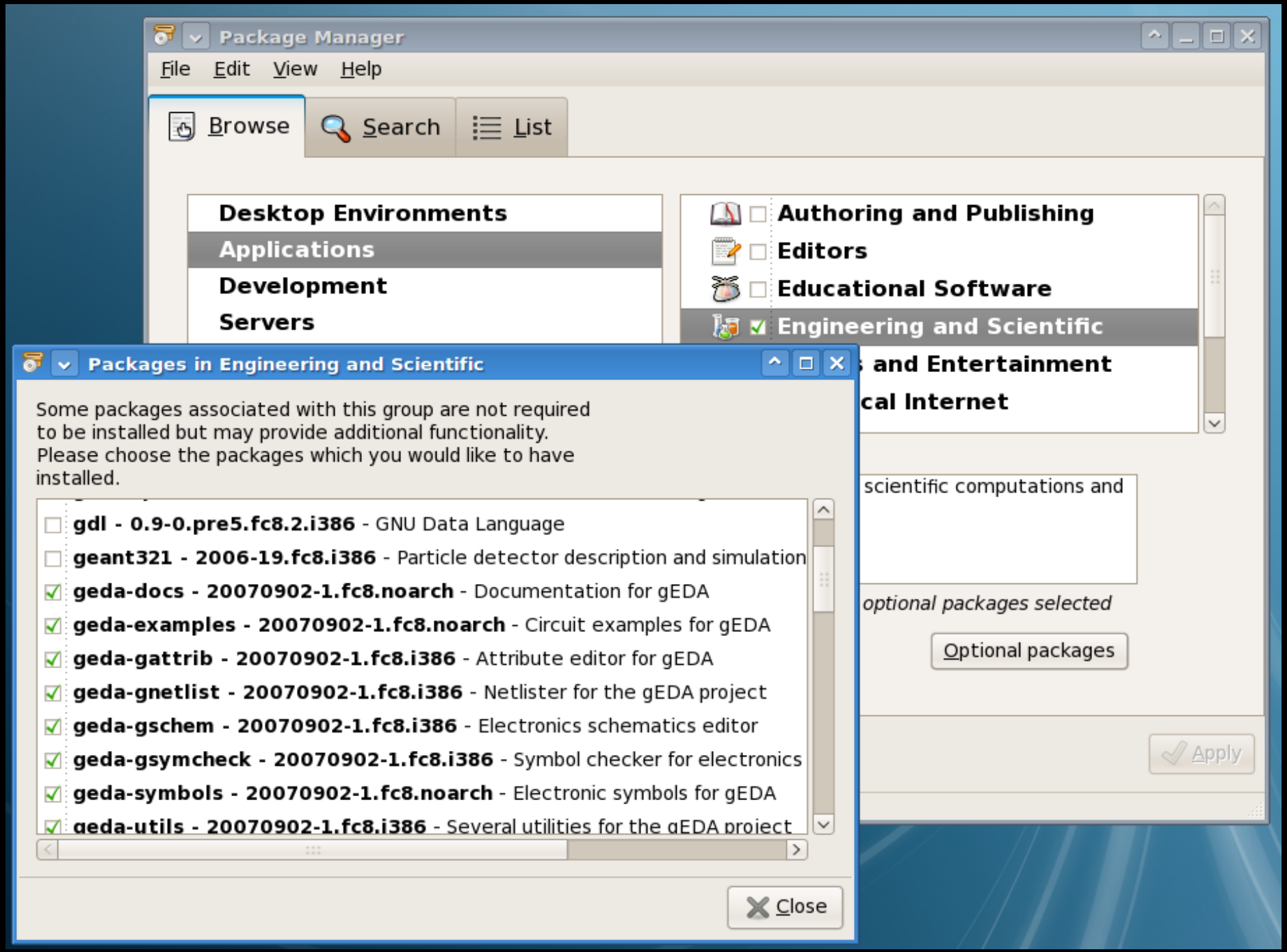
We have Man Power to provide Open Source Applications for everything you need.

Office	Science/Electronics	Games	Virtualisation / Servers	3D Desktop



[Quality & Security]

[Stable & well tested]


Package Manager
File Edit View Help
Browse Search List
Desktop Environments
Applications
Development
Servers
Authoring and Publishing
Editors
Educational Software
Engineering and Scientific
and Entertainment
cal Internet
scientific computations and
optional packages selected
Optional packages
Apply
Packages in Engineering and Scientific
Some packages associated with this group are not required
to be installed but may provide additional functionality.
Please choose the packages which you would like to have
installed.
gdl - 0.9-0.pre5.fc8.2.i386 - GNU Data Language
geant321 - 2006-19.fc8.i386 - Particle detector description and simulation
geda-docs - 20070902-1.fc8.noarch - Documentation for gEDA
geda-examples - 20070902-1.fc8.noarch - Circuit examples for gEDA
geda-gattrib - 20070902-1.fc8.i386 - Attribute editor for gEDA
geda-gnetlist - 20070902-1.fc8.i386 - Netlister for the gEDA project
geda-gschem - 20070902-1.fc8.i386 - Electronics schematics editor
geda-gsymcheck - 20070902-1.fc8.i386 - Symbol checker for electronics
geda-symbols - 20070902-1.fc8.noarch - Electronic symbols for gEDA
geda-utils - 20070902-1.fc8.i386 - Several utilities for the gEDA project
Close

Questions & Answers

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chitlesh@fedoraproject.org

http://chitlesh.fedorapeople.org

Standard Cell libraries

xooi21 standard cell family

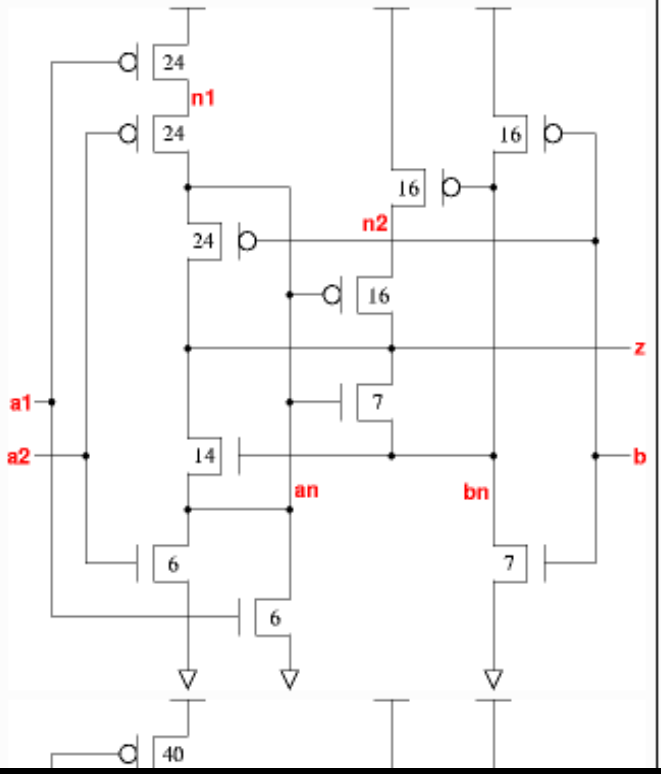
2-I/P exclusive NOR gate with 2-OR input

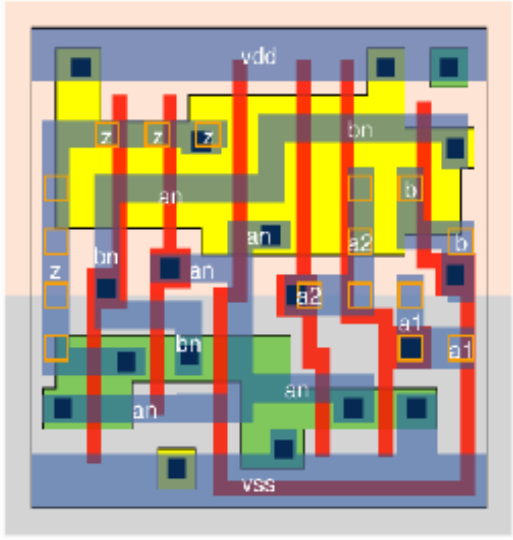
3 XNOR gates with OR gate input designed for minimum transistor count and hence smallest size. The OR gate is made by changing the inverter on the a input of a 2-XNOR gate into a 2-NOR gate. The Prop and Ramp delays below are the average of the inverting and non-inverting delays. The Synopsys Liberty format .LIB file has the correct delays for each case.

z:((a1+a2)^b)'	cell width			power		Generic 0.13um typical timing (ps & ps/fF), pin a2.				
				leakage	dynamic	tR=PropR+RampR×Load(fF), tF=PropF+RampF×Load(fF)				
vsclib013	gates	lambda	0.13um	nW	nW/MHz	PinCap	PropR	RampR	PropF	RampF
xooi21v0x05	3.0	72	3.96	0.87	19.7	3.7f	104	6.34	105	4.76
xooi21v0x1	4.0	96	5.28	1.52	29.6	6.0f	94	3.76	94	2.52
xooi21v0x2	6.7	160	8.80	2.73	56.8	11.2f	92	1.96	93	1.27

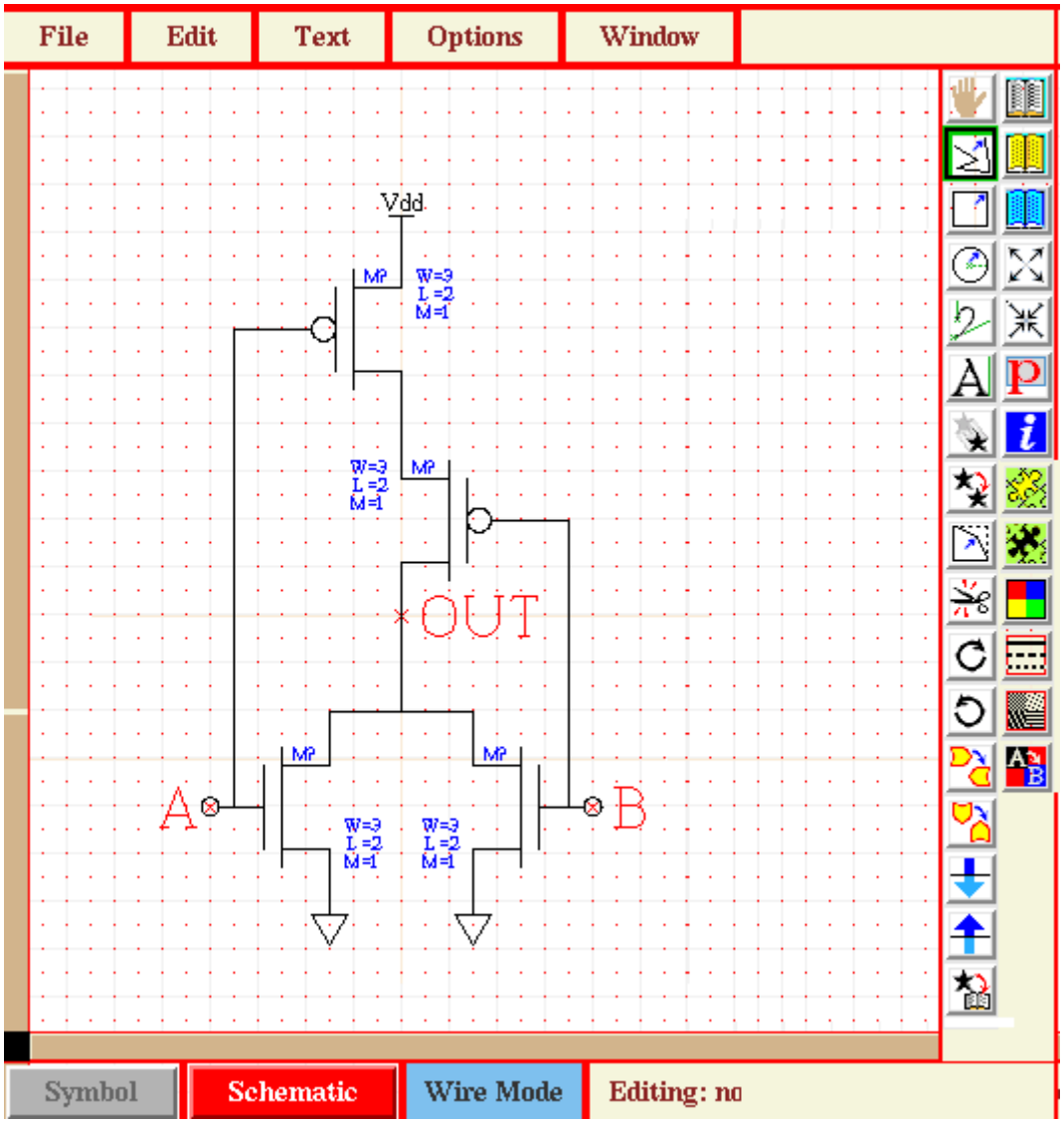
xooi21v0x05

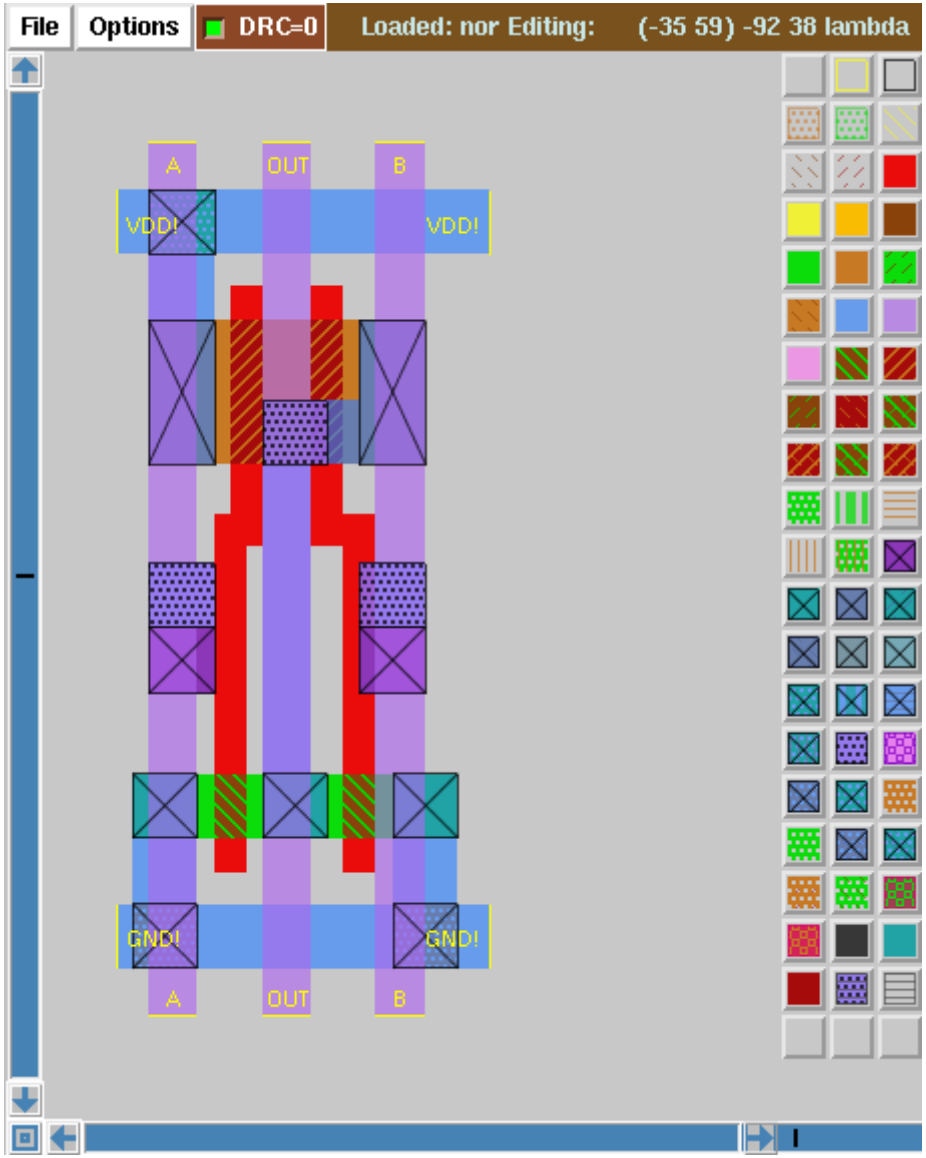
		Effort	
		FO4	Log.
a1	/\	2.35	1.97
	-	3.22	
	_		
a2	/\	2.21	1.95
	-	3.13	
	_		
b	/\	2.41	3.06
	-	2.74	
	_		

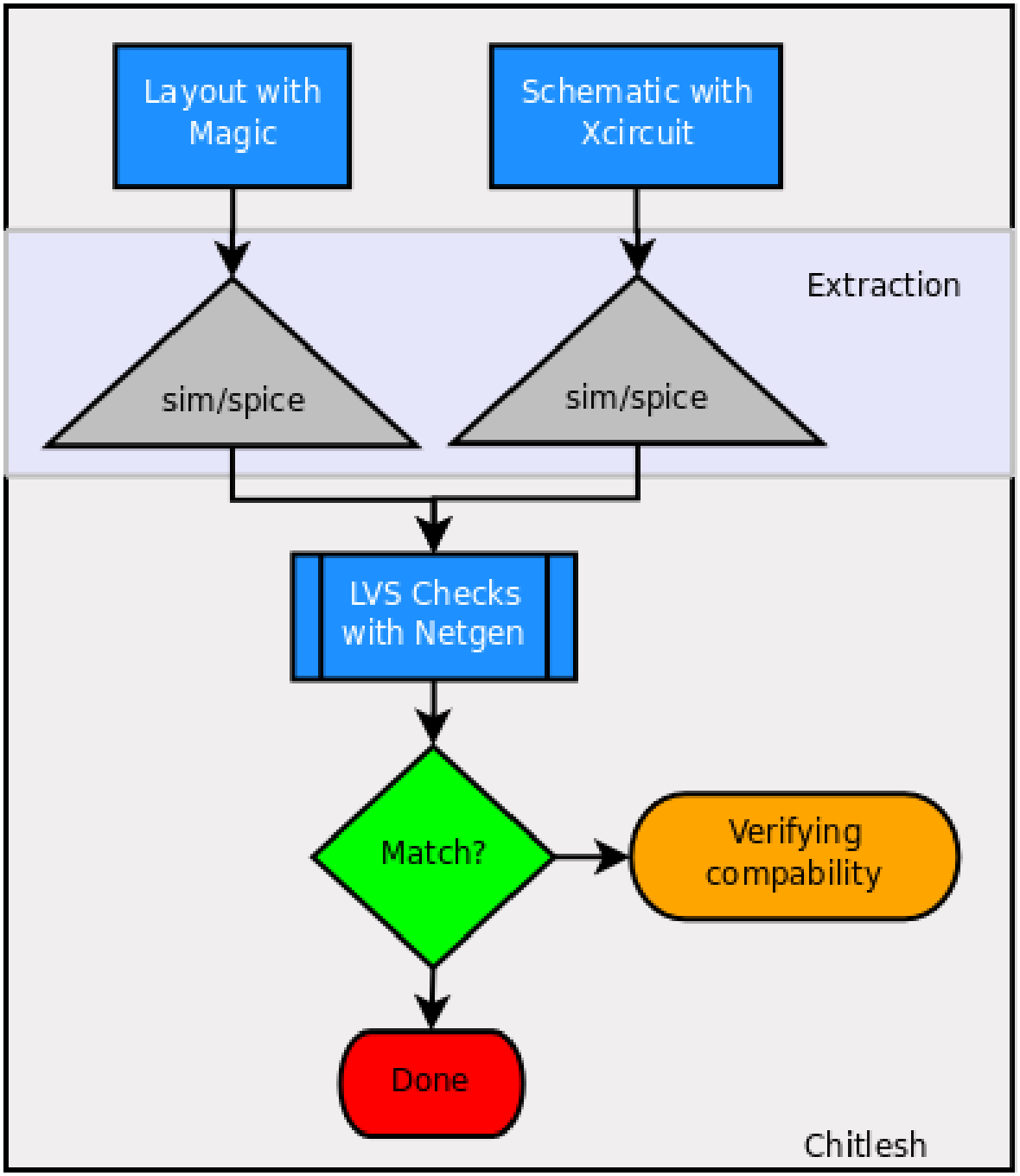


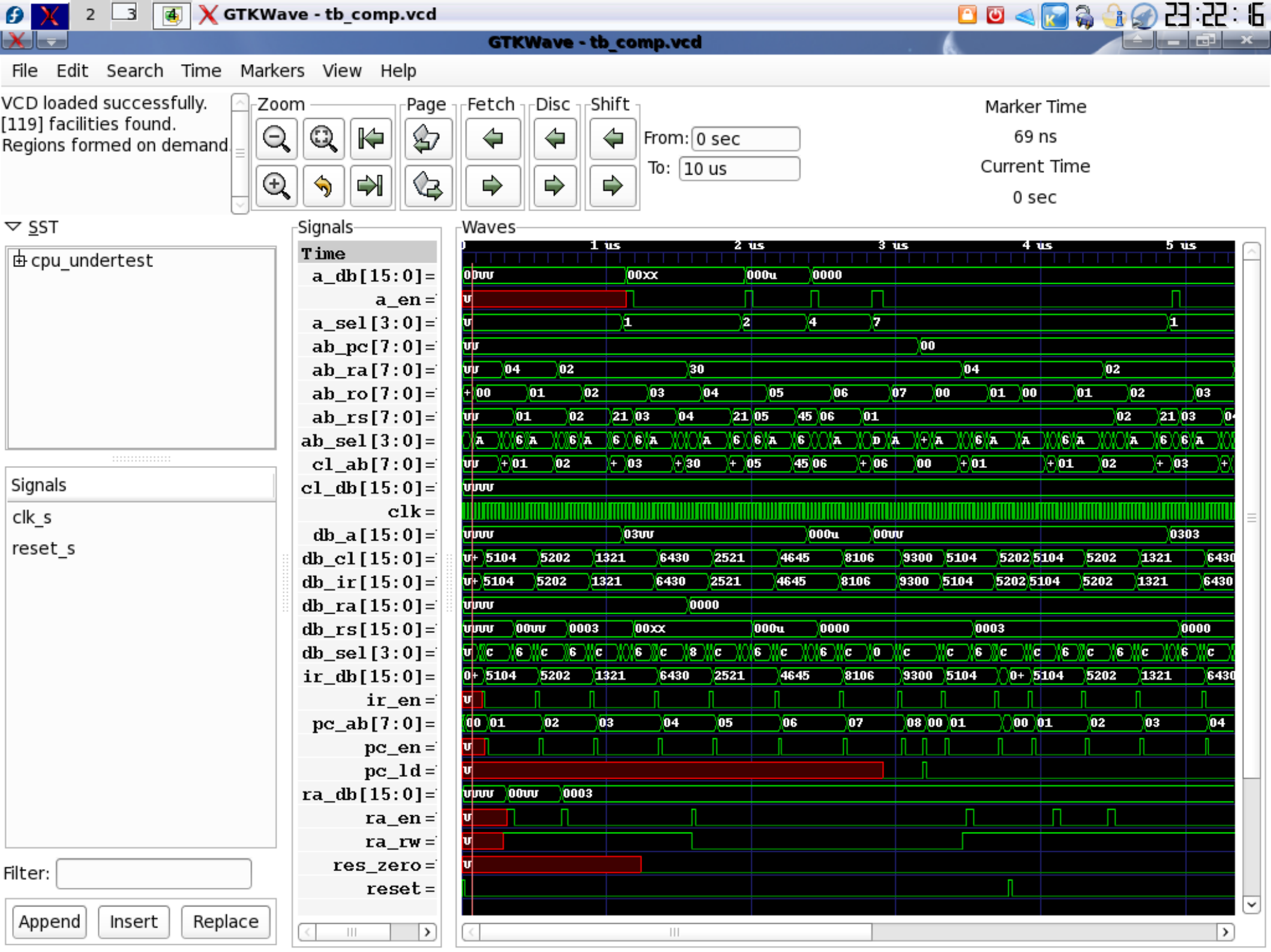


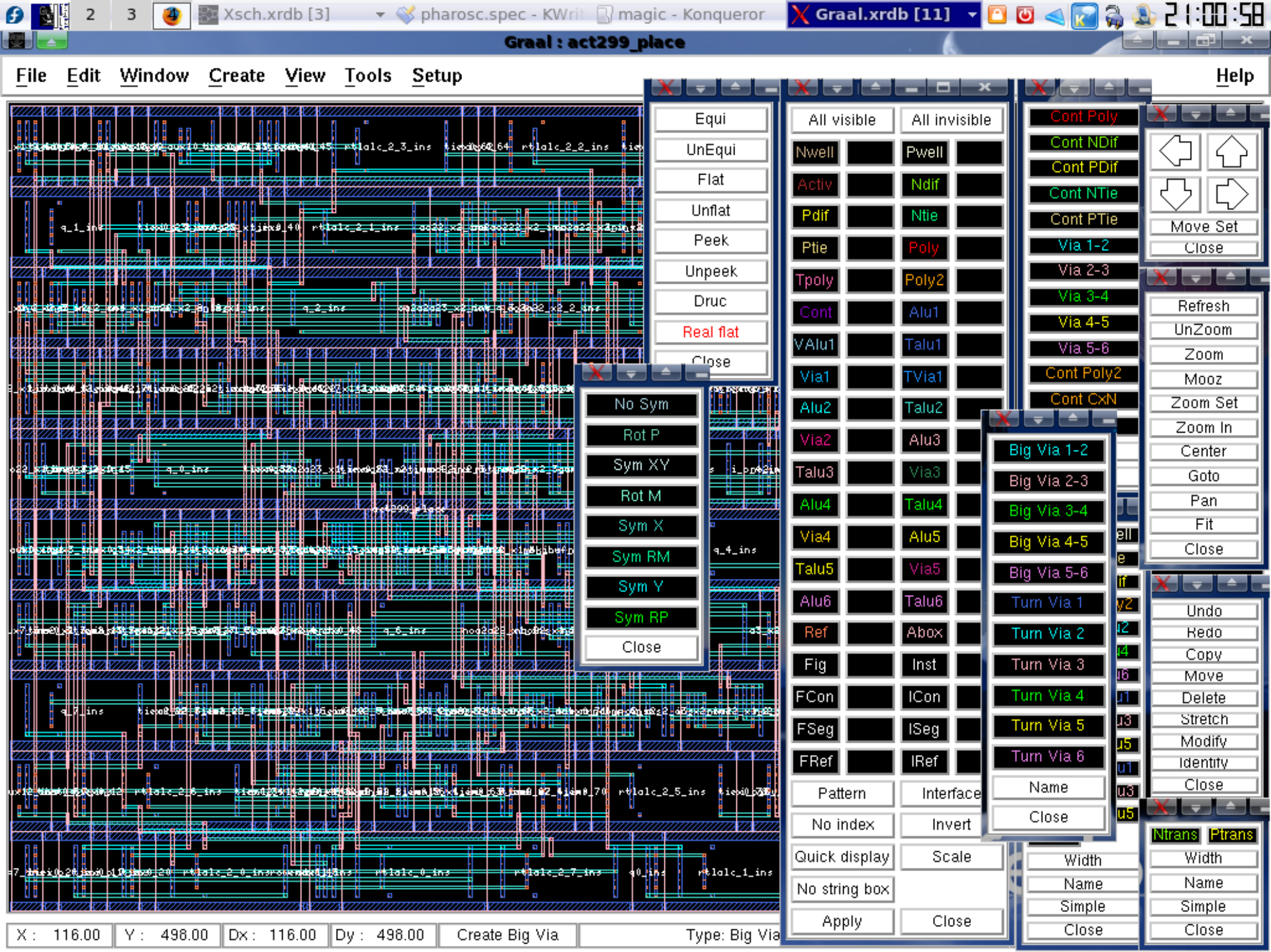

location: 0.7 -3.5 -8.3 fps: 147.1
look_at: 0.8 -3.2 -7.4
Zoom
Rotate

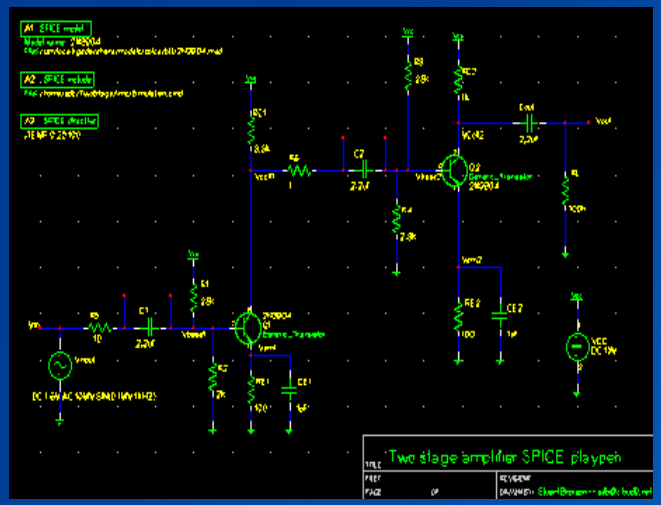

File
Edit
Text
Options
Window
Vdd
MP
W=3
L=2
M=1
OUT
A
B
Symbol
Schematic
Wire Mode
Editing: no

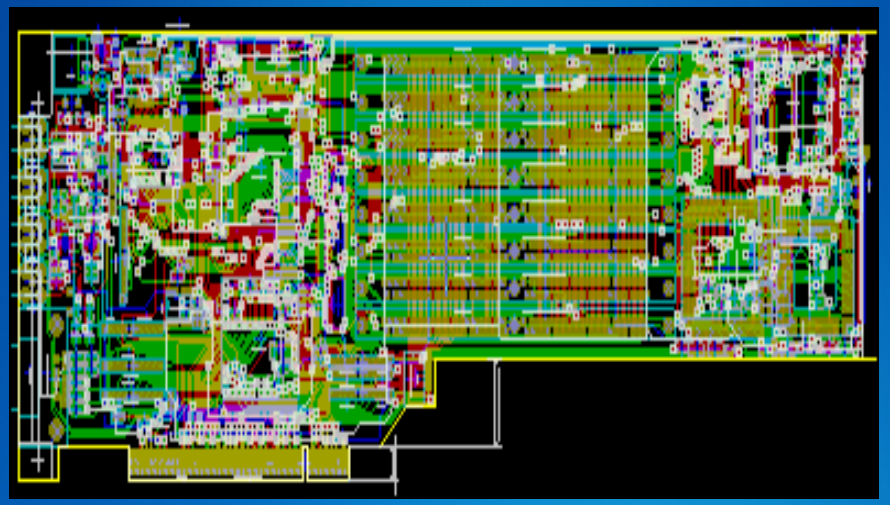

File
Options
DRC=0
Loaded: nor Editing:
(-35 59) -92 38 lambda
A
OUT
B
VDD!
VDD!
GND!
GND!
A
OUT
B

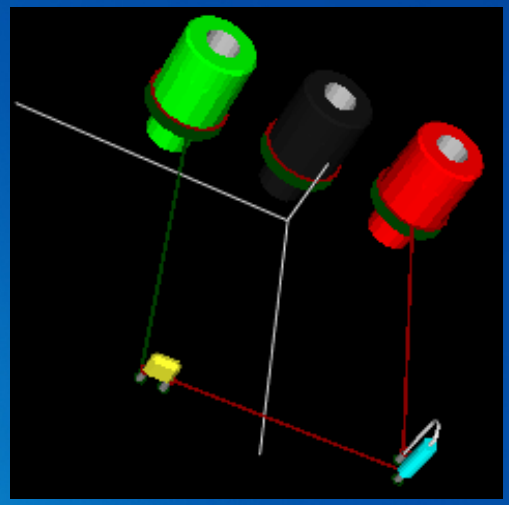

Layout with Magic
Schematic with Xcircuit
Extraction
sim/spice
sim/spice
LVS Checks with Netgen
Match?
Verifying compability
Done
Chitlesh


GTKWave - tb_comp.vcd
GTKWave - tb_comp.vcd
File Edit Search Time Markers View Help
VCD loaded successfully.
[119] facilities found.
Regions formed on demand
Zoom
Page
Fetch
Disc
Shift
From: 0 sec
To: 10 us
Marker Time
69 ns
Current Time
0 sec
SST
cpu_undertest
Signals
clk_s
reset_s
Filter:
Append
Insert
Replace
Signals
Time
a_db[15:0]
a_en
a_sel[3:0]
ab_pc[7:0]
ab_ra[7:0]
ab_ro[7:0]
ab_rs[7:0]
ab_sel[3:0]
cl_ab[7:0]
cl_db[15:0]
clk
db_a[15:0]
db_cl[15:0]
db_ir[15:0]
db_ra[15:0]
db_rs[15:0]
db_sel[3:0]
ir_db[15:0]
ir_en
pc_ab[7:0]
pc_en
pc_ld
ra_db[15:0]
ra_en
ra_rw
res_zero
reset
Waves
1 us
2 us
3 us
4 us
5 us


Graal : act299_place
File
Edit
Window
Create
View
Tools
Setup
Help
Equi
UnEqui
Flat
Unflat
Peek
Unpeek
Druc
Real flat
Close
No Sym
Rot P
Sym XY
Rot M
Sym X
Sym RM
Sym Y
Sym RP
Close
All visible
All invisible
Nwell
Pwell
Activ
Ndif
Pdif
Ntie
Ptie
Poly
Tpoly
Poly2
Cont
Alu1
VAlu1
Talu1
Via1
TVia1
Alu2
Talu2
Via2
Alu3
Talu3
Via3
Alu4
Talu4
Via4
Alu5
Talu5
Via5
Alu6
Talu6
Ref
Abox
Fig
Inst
FCon
ICon
FSeg
ISeg
FRef
IRef
Pattern
Interface
No index
Invert
Quick display
Scale
No string box
Apply
Close
Cont Poly
Cont NDif
Cont PDif
Cont NTie
Cont PTie
Via 1-2
Via 2-3
Via 3-4
Via 4-5
Via 5-6
Cont Poly2
Cont CxN
Big Via 1-2
Big Via 2-3
Big Via 3-4
Big Via 4-5
Big Via 5-6
Turn Via 1
Turn Via 2
Turn Via 3
Turn Via 4
Turn Via 5
Turn Via 6
Name
Close
Move Set
Close
Refresh
UnZoom
Zoom
Mooz
Zoom Set
Zoom In
Center
Goto
Pan
Fit
Close
Undo
Redo
Copy
Move
Delete
Stretch
Modify
Identify
Close
Ntrans
Ptrans
Width
Name
Simple
Close
Width
Name
Simple
Close
X : 116.00
Y : 498.00
Dx : 116.00
Dy : 498.00
Create Big Via
Type: Big Via



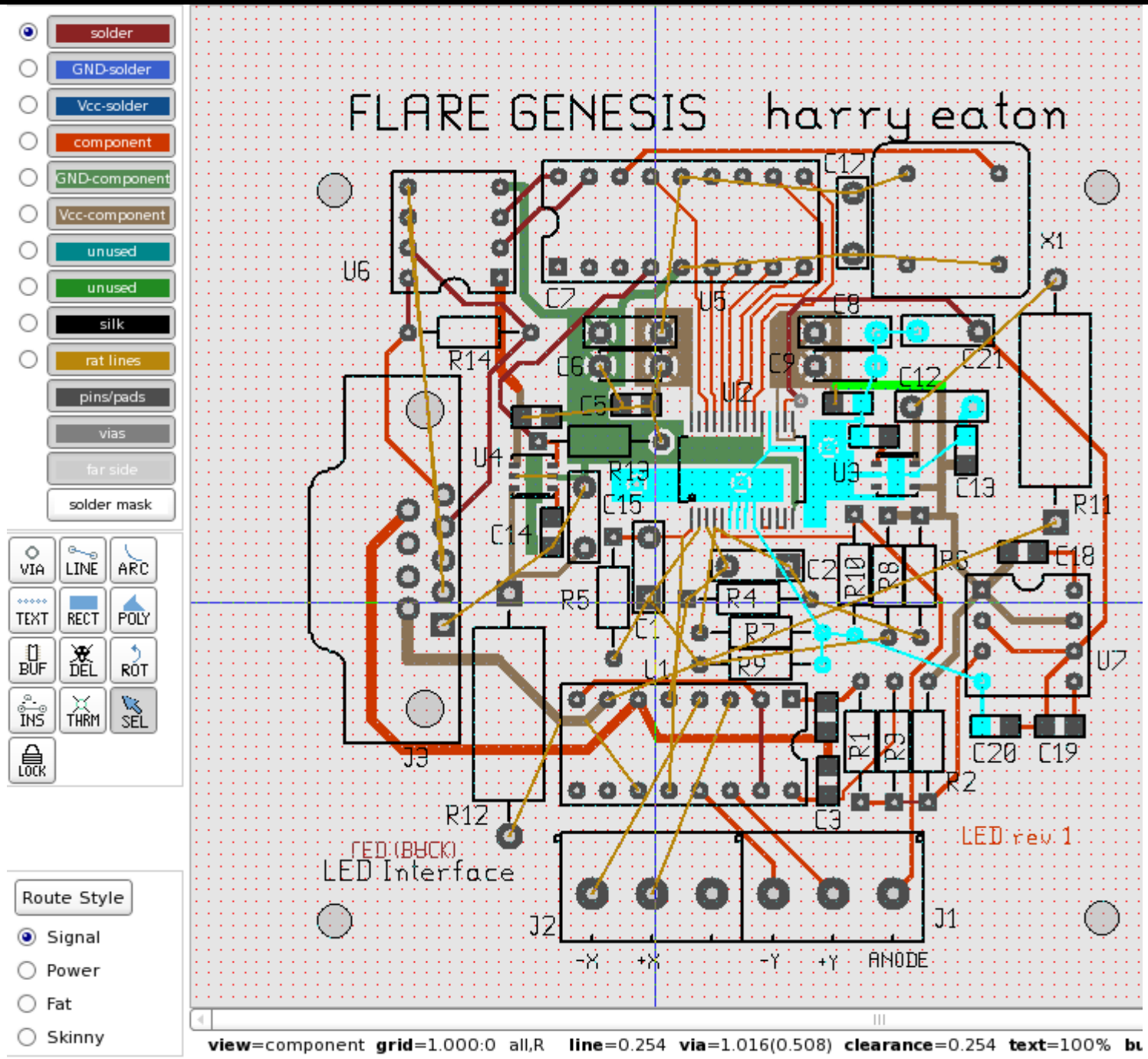




Schematic Capture to Netlist

Hierarchy

Circuit Simulations : spice, BSIM + EKV implementation


solder
GND-solder
Vcc-solder
component
GND-component
Vcc-component
unused
unused
silk
rat lines
pins/pads
vias
far side
solder mask
VIA
LINE
ARC
TEXT
RECT
POLY
BUF
DEL
ROT
INS
THRM
SEL
LOCK
Route Style
Signal
Power
Fat
Skinny
FLARE GENESIS harry eaton
LED Interface
LED rev 1
-X
+X
-Y
+Y
ANODE
view=component grid=1.000:0 all,R line=0.254 via=1.016(0.508) clearance=0.254 text=100%


The fedora team