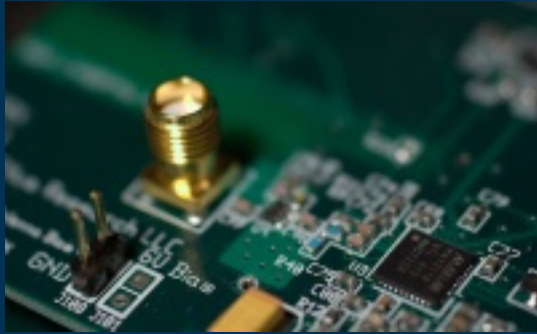The Fedora Project is out front for you, leading the advancement of free, open software and content.

fedora
electronic lab 10

Community Leader in opensource EDA deployment

Reduce deployment time

Focus on your design

Increase productivity

analog, digital, RTL, arm, **vhdl**, spice, VLSI, **ASIC**, microcontroller, transistor, **standard cells**, BSIM, **simulation**, verilog, layout, **PCB**, synthesis, design flows, DRC, schematic, PyCell, LVS, gerber, assembly, finite state machine, **interoperobality**, avr, **embedded**, program,....

http://chitlesh.fedorapeople.org/FEL
fedora-electronic-lab-list@redhat.com

Design, Simulate & Program Electronics

Feel the need to deploy a quality-class Linux distribution for electronic design and simulation !!

fedora leads in innovation, features, community development. Aside from better hardware support, Fedora strives to give you the best productive experience you may have with opensource software.

About

Started as providing a few handful set of design tools 3 years ago, now Fedora Electronic Lab is a matured simulation platform for **Micro-Nano Electronics Engineering and Embedded Systems.**

Now fedora has more than 9.5 million users around the world. Fedora Electronic Lab, a subset of Fedora, is also available for free has already been adopted by many small universities and hobbyists.

Design Tools for

– Analog/Digital Simulation

– Circuit Simulation

– Verification and Documentations

– Hardware Development

– Micro Controller Programming

– Embedded Systems Development
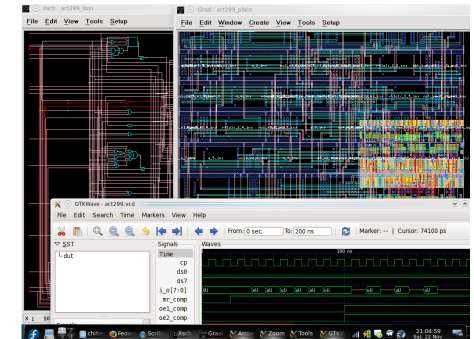
Introduces:

– tools for Application-Specific Integrated Circuit (ASIC) Design Flow process.
– extra standard cell libraries supporting a feature size of 0.13μm.
– extracted spice decks which can be simulated with any spice simulators.
– interoperability between packages to achieve different design flows.

VLSI Design Layout & Checks

Includes
- A continuous DRC that operates in background and maintains an up-to-date picture of violations.
- A hierarchical circuit extractor that only re-extracts portions of the circuit that have changed.
- Plowing that permits interactive stretching and compaction.
- Routing tools that work under and around existing connections.
- Logs and corner stitching to achieve efficient implementations.

Dedicated to training in sub-micron CMOS VLSI design
with full editing facilities.

Supports technology files by the MOSIS foundry service.

Switch-level simulation of the layout,
by considering transistors as ideal switches,
or using RC time constants to predict the relative timing of events
through extracted capacitance and lumped resistance values.

Ensures that layout connectivity matches the logical design represented by the schematic or netlist before tapeout by automatically
- extracting devices and nets formed across layout hierarchy and,
- comparing them to the schematic netlist. (LVS)

Generates GDS II stream format and Caltech Intermediate Form (CIF) from a given layout.

Achievement : Thick-film circuit layout using the Magic layout editor.
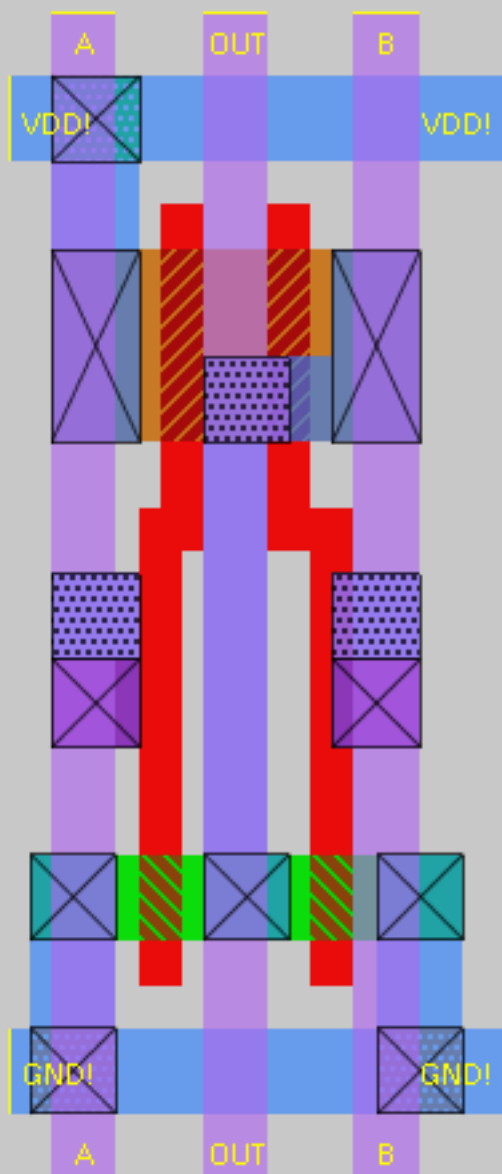
A HDL simulation environment that enables you to verify the functional and timing models of your design.

Thus, your Design teams can focus on improving existing methodologies with tools that scale across multiple levels of abstraction and design complexity.

Achievements:

Successfully compiled and run
— a DLX processor and
— a LEON1 SPARC processor.

Automatic layout generation from VHDL description via desired standard cell libraries.

Key Features:

Supports both VHDL and Verilog designs.

Implementation of the VHDL language in accordance to the
   o IEEE 1076-1987 standard
   o IEEE 1076-1993 standard
   o the protected types of VHDL00
      (aka IEEE 1076a or IEEE 1076-2000)
   o and non-standard third party libraries.

VPI functionality.

Export signals to a VCD file or a GHW file for visual inspection with a waveform viewer.

Pretty printing or cross references generation in HTML.

Makefile generation for any component in a design.

A graphical waveform viewer.

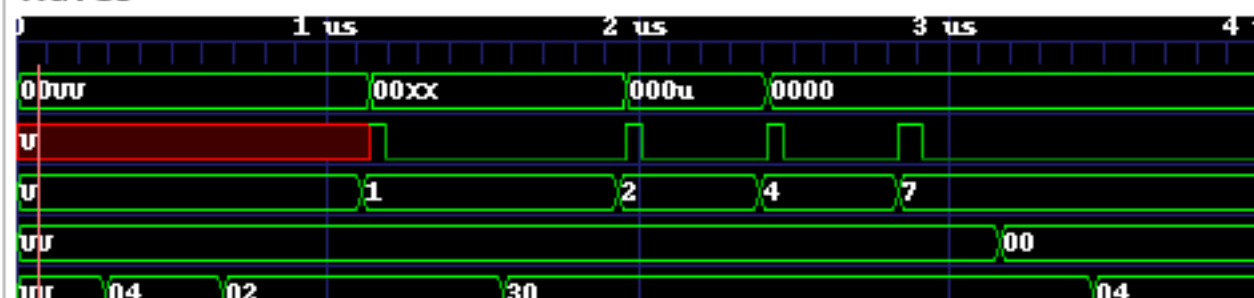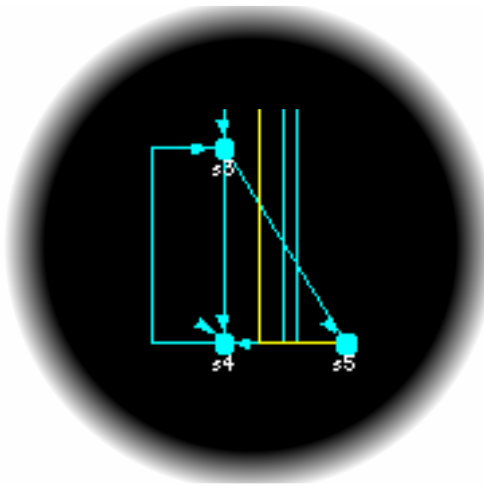A Verilog simulator and synthesis tool for IEEE 1364-2001 standard.

RTL and logic synthesis design flows.

Automatic schematic generation
VHDL compilation and simulation
Finite State Machines (FSM)
Model checking and formal proof

RTL and Logic synthesis,
Data-Path compilation,
Macro-cells generation,
Symbolic Pad cells
Design rules checking,....

Physical optimization and layout design flows.
Complete RTL to CIF and GDSII flows.
7 extra standard cells up to a feature size of 0.13µm
Read/write standard ins/outs including
Verilog® and VHDL.

Place and route,
Layout edition,
Automatic Layout generation
Netlist extraction and verification
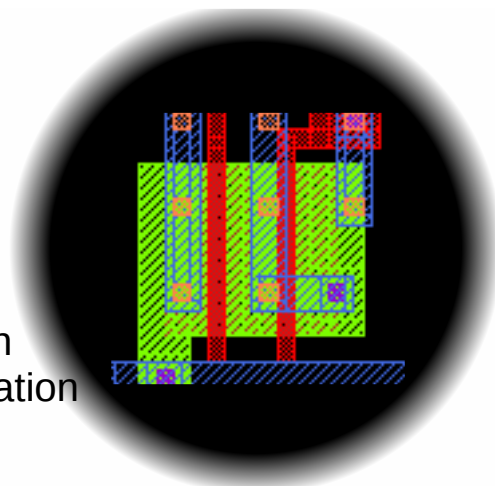
Creates a POV-Ray (3D view)
scene description file of the
GDSII data.

Circuit   Simulation

This simulation lab enables design engineers to simulate their schematics.
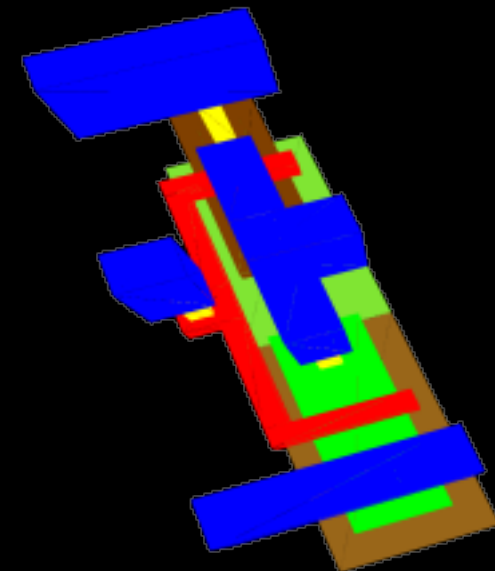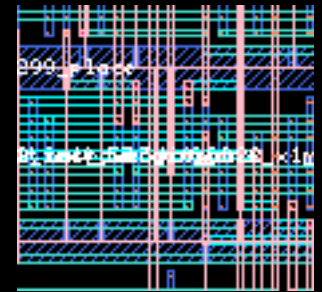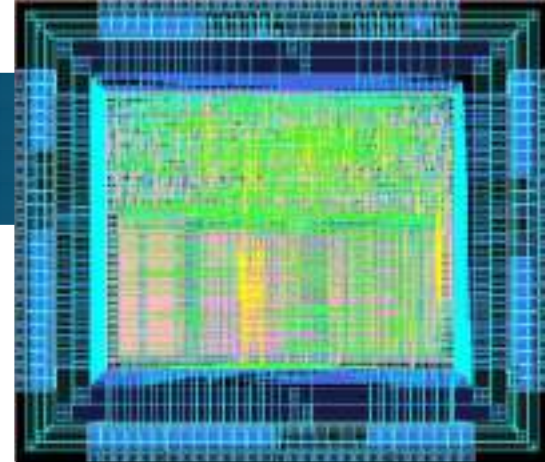
– General Purpose Circuit Simulators
   o Nonlinear AC/DC analysis
   o Transient, Fourier analysis
   o S-parameter and harmonic balance analysis
– Beyond Spice capabilities: Level 49, BSIMv3 and EKV implementations
– Multi-lingual, ablilty to mimic different variants of spice,
   and also supporting the newer languages like Verilog-AMS
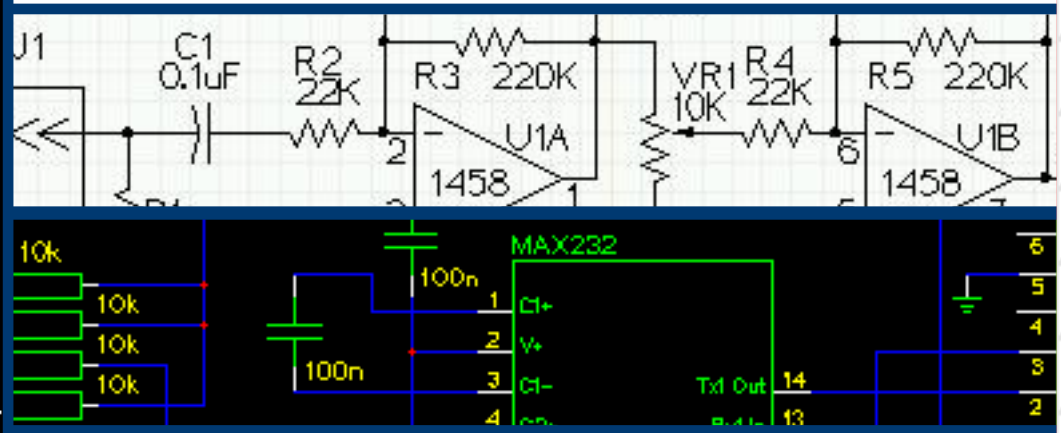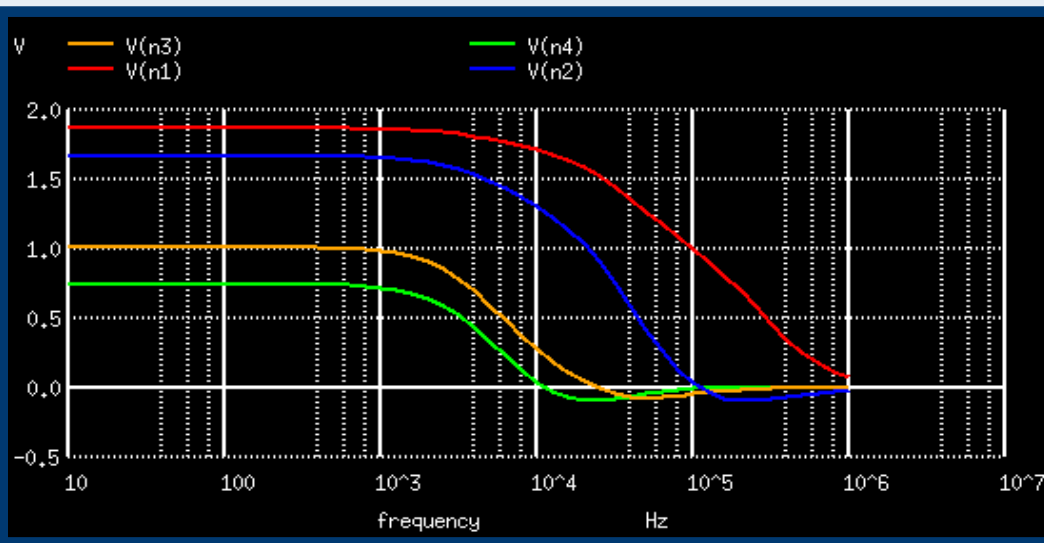
– Draws publishable-quality electrical circuit schematic diagrams.

– Circuit components can be retrieved from libraries which are fully editable.

– Easy-to-use GUI with TCL interface or GTK interface.

PCB Layout Design

A professional-quality **printed circuit board design environment** along with :
schematic capture, simulation, prototyping attribute management,
bill of materials (BOM) generation and netlisting into over 20 netlist
formats.

Includes a rats nest feature, design rule checking, and can provide industry
standard RS-274-X (Gerber), NC drill, and centroid data (X-Y data)
output for use in the board fabrication and assembly process.

Offers high end features such as an autorouter and trace optimizer,
which can tremendously reduce layout time.

Creates PCB of up to 8 layers with an unlimited number of components and
nets.

Includes a viewer for Gerber files (RS274X),
which supports NC-drill and Excellon formats.

µController Programming

Supported compilers :
    the Small Device C Compiler, the GNU PIC Utilities, the PICC compilers,
    the PIC30 toolchain, the C18 compiler, the JAL and JALV2 compilers,
    the CSC compiler, and the Boost compilers.

Ease to use IDEs for microcontrollers circuit design, simulation and programmation to serial, parallel and USB ports.
IDE includes an oscilloscope and a flowchart integration.

Supported debuggers :   ICD2 and GPSim.
Supported programmers :
    ICD2, PICkit1 and PICkit2 and PicStart+ programmers.

Supports 8051 and AVR and Binutils for SPU on IBM Cell processors.

Arm and AVR Development System

Supports the Atmel's STK500 and the PPI (parallel port interface) programmer types.

Includes
    – Cross compilers and Programmers
    – a Universal In-System Programmer for Atmel AVR and 8051
    – a Program for interfacing the Atmel JTAG ICE to GDB

Small Device C Compiler

Embedded Systems Development

fedora

electronic lab

Fedora is a Linux-based operating system. Fedora is always free for anyone to use, modify, and distribute.

Fedora Electronic Laboratory (FEL) provides a complete electronic laboratory setup with reliable open source design tools as well as project management tools such as spreadsheet, mindmap, gantt diagram....

It can be downloaded freely as a LiveDVD via torrent.

Download the latest version 10.

All Fedora Electronic Lab packages can be freely installed via yum from official repositories.

website :

http://chitlesh.fedorapeople.org/FEL

technical support :

Fedora Electronic Lab Mailing List

contact:

Chitlesh GOORAH
(Fedora Electronic Lab Architect)

Fedora Embedded SIG

Fedora SciTech SIG