Design, Simulate and Program electronics.

fedora *electronic lab*

Beyond software

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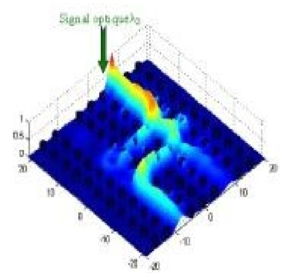
Fosdem-Brussels
7-8 February 2009

Fedora Project

has Man Power to provide Open Source Applications for everything you need.

Office	Science/Electronics	Games	Virtualisation / Servers	3D Desktop



[Quality & Security]

[Stable & well tested]

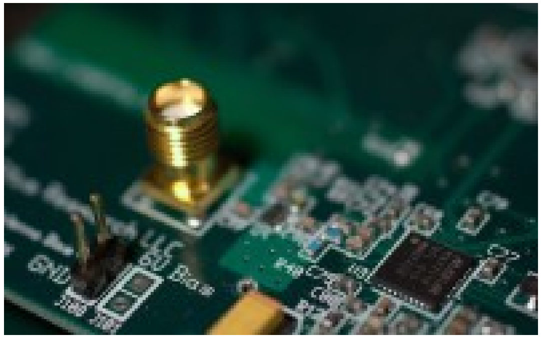
[fedora's Guiding Principles]

Encourage Collaborative Development

Release Early, Release Often

Mutual Benefit of Community and Company

Importance of Upstream



[Fedora Electronic Lab]

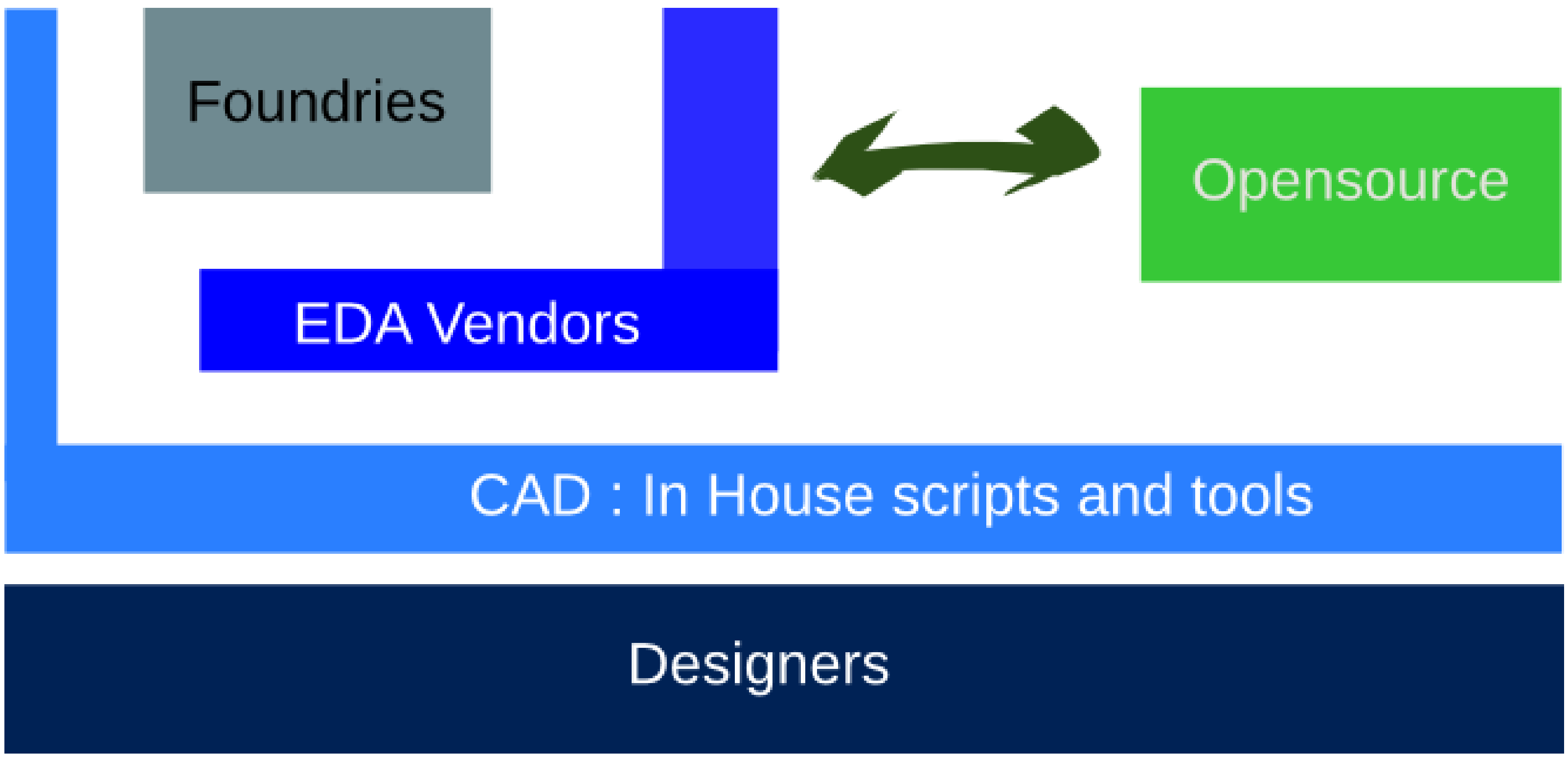
An opensource Design and Simulation platform For Electronics

A one-stop linux distribution for hardware design

Marketing means for opensource EDA developers (Networking)

XUROPA℠

Identifying a Problem to solve !



Electronic Designers Problems

Approx. 6 month design development cycle

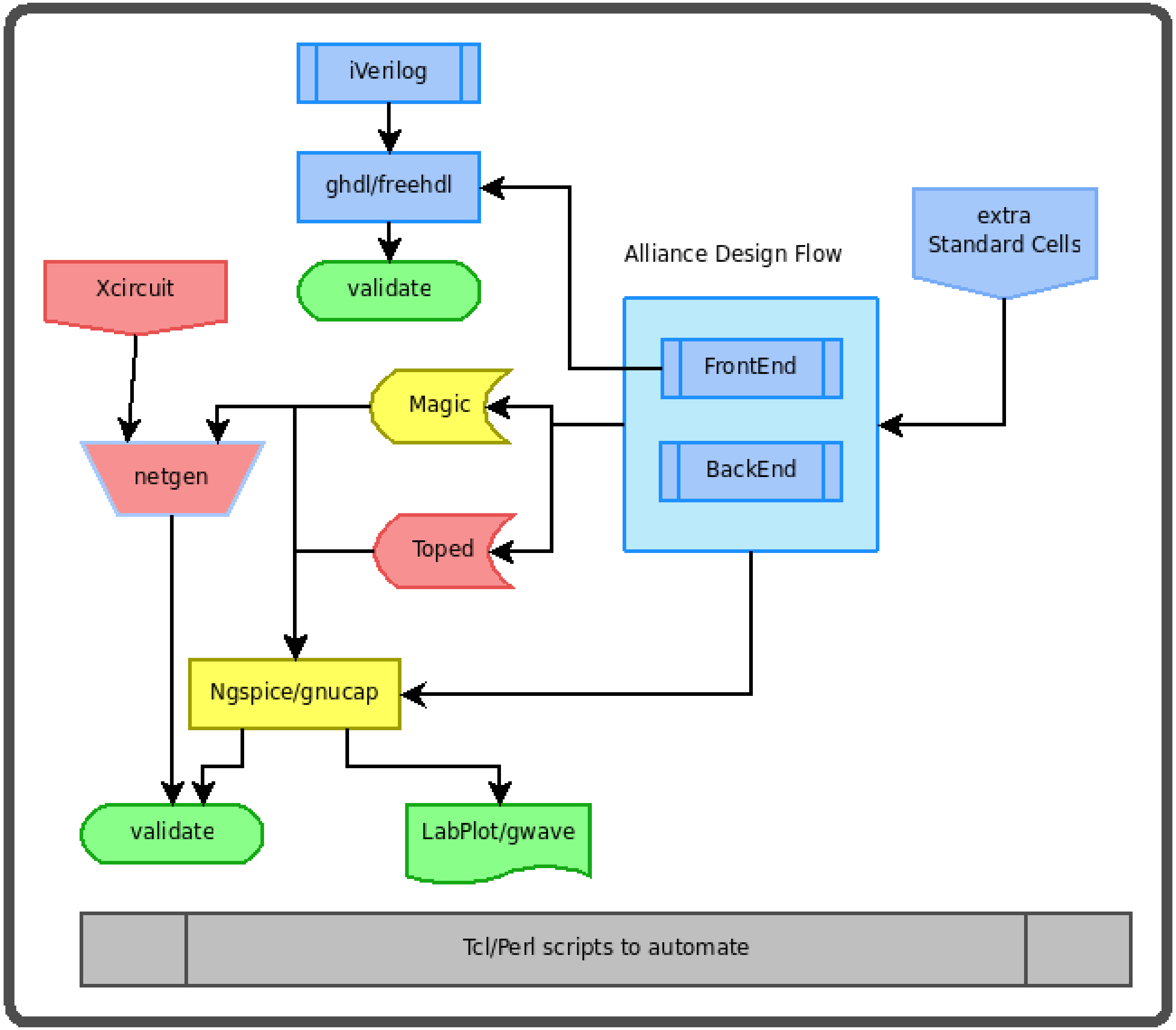
Tackling Design Complexity

Lower Power, Lower Cost and Smaller Space

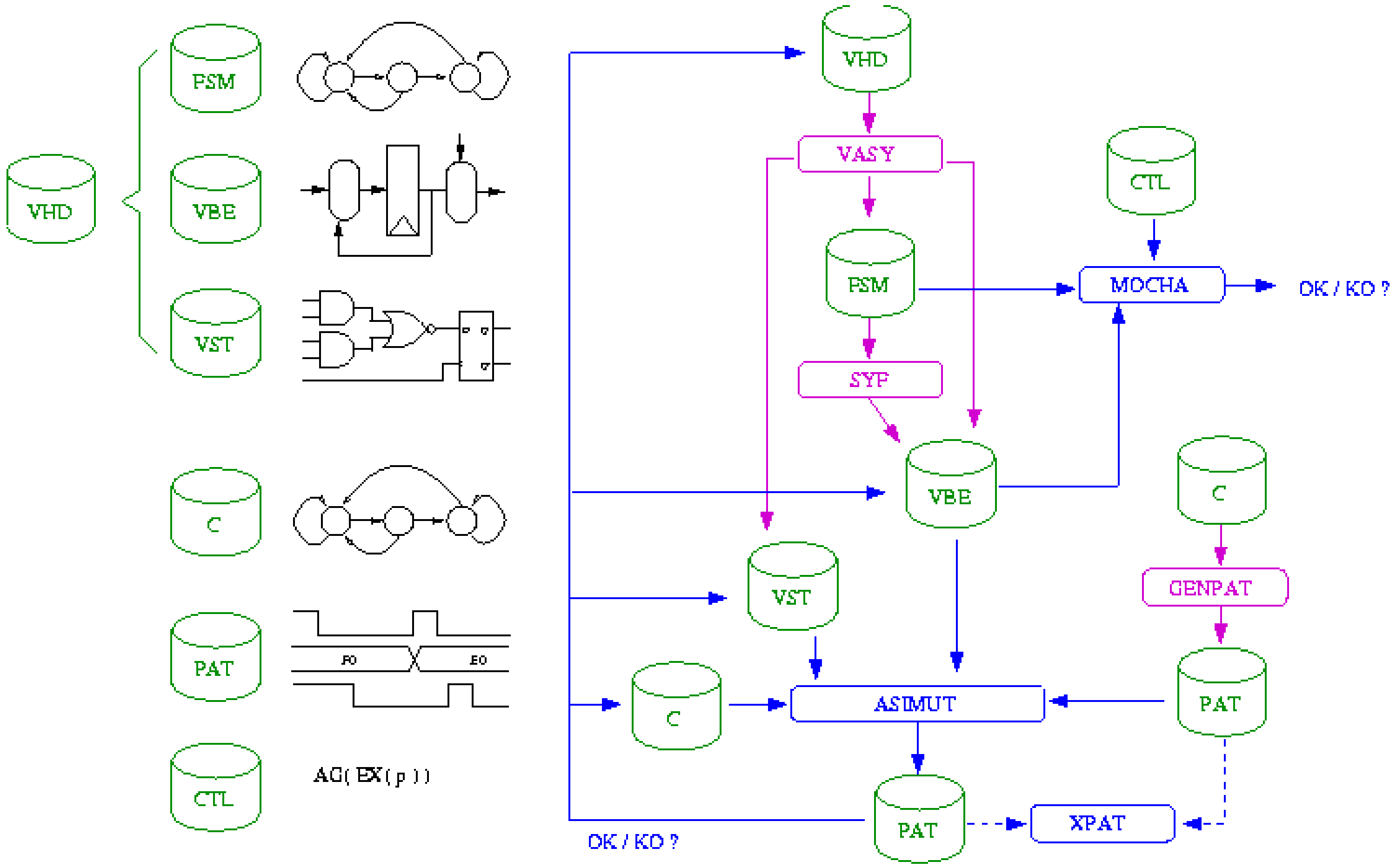
EDA Industry's neck squeezed in 2008

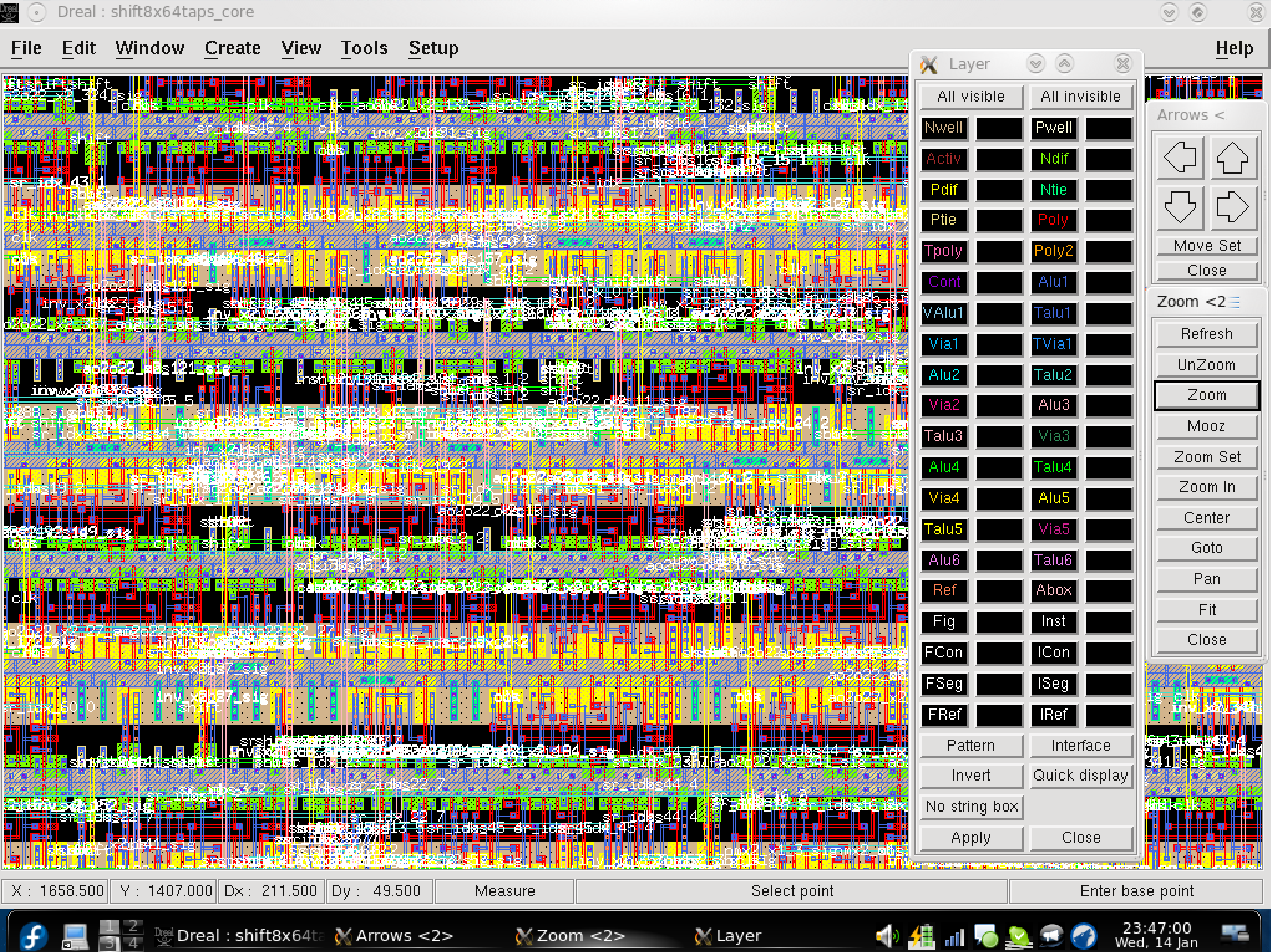
Management (digital/analog) IP Portfolio

A basic Design Flow



Example of RTL Synthesis versus scripting




Dreal : shift8x64taps_core
File
Edit
Window
Create
View
Tools
Setup
Help
Layer
All visible
All invisible
Nwell
Pwell
Activ
Ndif
Pdif
Ntie
Ptie
Poly
Tpoly
Poly2
Cont
Alu1
VAlu1
Talu1
Via1
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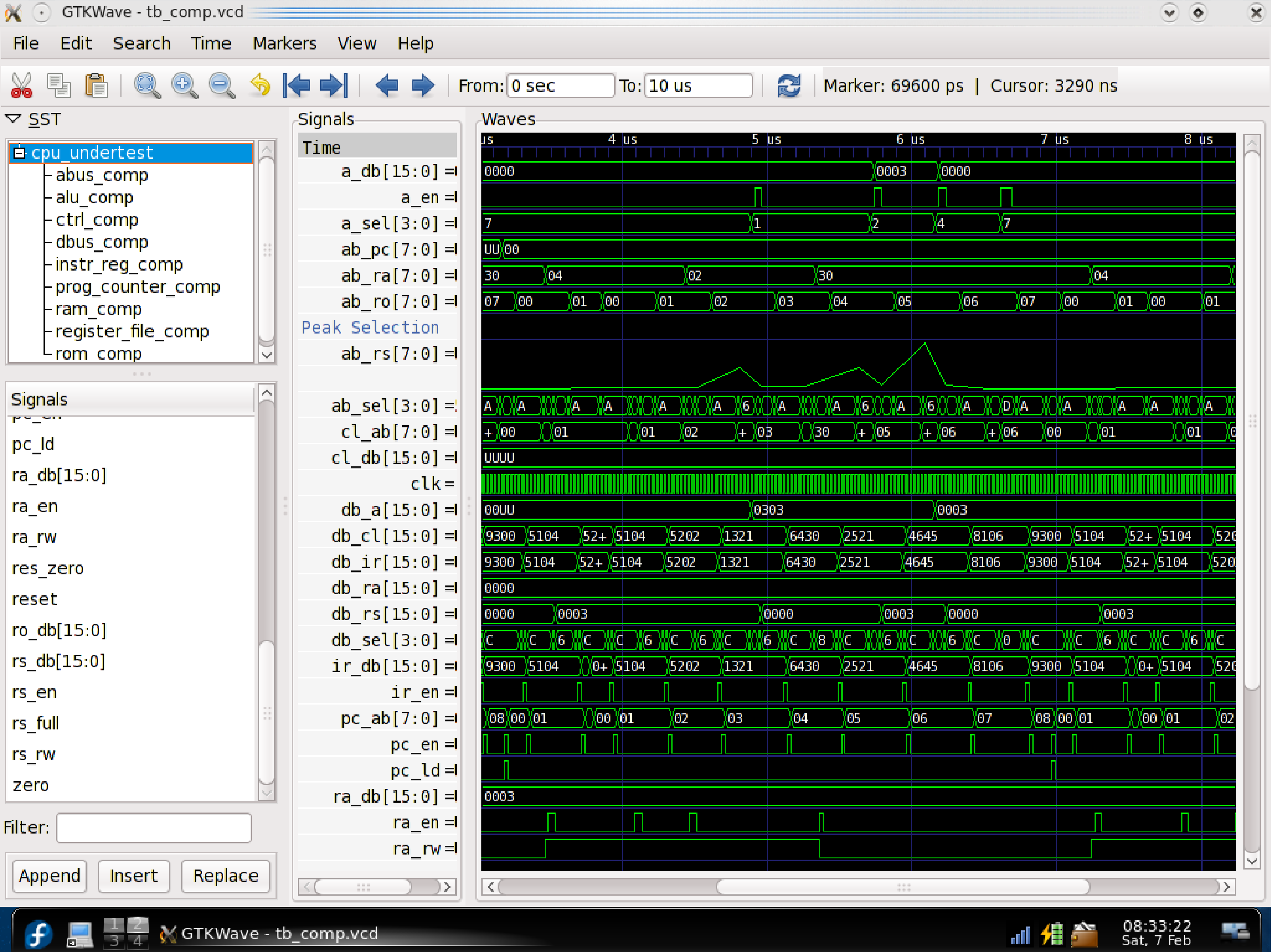
Via5
Alu6
Talu6
Ref
Abox
Fig
Inst
FCon
ICon
FSeg
ISeg
FRef
IRef
Pattern
Interface
Invert
Quick display
No string box
Apply
Close
Arrows <
Move Set
Close
Zoom <2
Refresh
UnZoom
Zoom
Mooz
Zoom Set
Zoom In
Center
Goto
Pan
Fit
Close
X : 1658.500
Y : 1407.000
Dx : 211.500
Dy : 49.500
Measure
Select point
Enter base point
Dreal : shift8x64t
Arrows <2>
Zoom <2>
Layer
23:47:00
Wed, 14 Jan

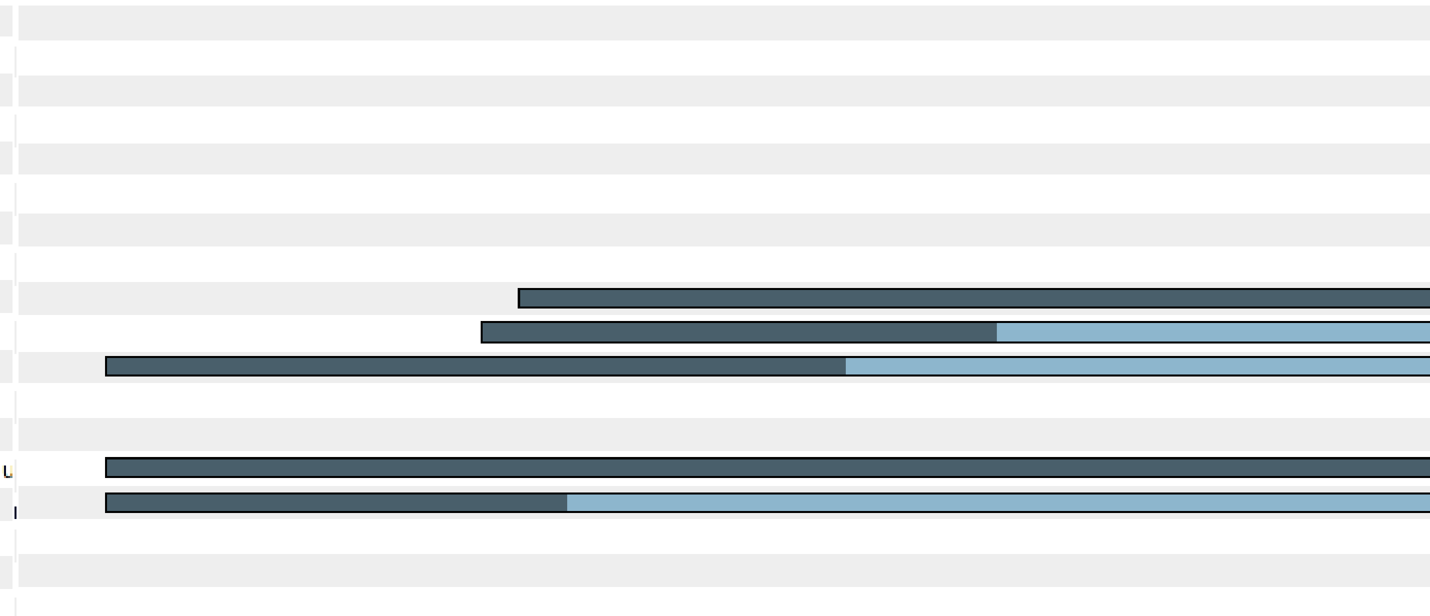

GTKWave - tb_comp.vcd
File
Edit
Search
Time
Markers
View
Help
From: 0 sec
To: 10 us
Marker: 69600 ps | Cursor: 3290 ns
SST
cpu_undertest
abus_comp
alu_comp
ctrl_comp
dbus_comp
instr_reg_comp
prog_counter_comp
ram_comp
register_file_comp
rom_comp
Signals
pc_ld
ra_db[15:0]
ra_en
ra_rw
res_zero
reset
ro_db[15:0]
rs_db[15:0]
rs_en
rs_full
rs_rw
zero
Filter:
Append
Insert
Replace
Signals
Time
a_db[15:0]
a_en
a_sel[3:0]
ab_pc[7:0]
ab_ra[7:0]
ab_ro[7:0]
Peak Selection
ab_rs[7:0]
ab_sel[3:0]
cl_ab[7:0]
cl_db[15:0]
clk
db_a[15:0]
db_cl[15:0]
db_ir[15:0]
db_ra[15:0]
db_rs[15:0]
db_sel[3:0]
ir_db[15:0]
ir_en
pc_ab[7:0]
pc_en
pc_ld
ra_db[15:0]
ra_en
ra_rw
Waves
4 us
5 us
6 us
7 us
8 us
GTKWave - tb_comp.vcd
08:33:22
Sat, 7 Feb

How would you shape FEL Development ?

Fedora Electronic Lab 11 Development Timeline - Planner - Mozilla Firefox

http://chitlesh.fedorapeople.org/FEL/devel/FEL_devel_timeline.html

3.3.6.2	Fedora
3.3.7	**Documentation**
3.3.7.1	wiki
3.3.7.2	promotional materials
3.3.7.3	hosted repository
3.3.7.4	aid edu-spin
3.3.7.5	FOSDEM Flyer
3.3.7.6	Xuropa Online Booth
3.3.8	**Upstream**
3.3.8.1	geda/gerbv
3.3.8.2	toped
3.3.8.3	pcb
3.3.8.4	verilator vs systemperl
3.3.8.5	Ktechlab
3.3.8.6	Promote Opensource EDA commu
3.3.9	Upstream talks
3.4	**FEL11 Releases**
3.4.1	LiveDVD tuning
4	FEL12



Tasks

WBS	Name	Start	Finish	Work	Priority	Complete	Cost	Notes
1	**FEL10**	Nov 3	Nov 26	19d				FEL 10 Cambridge Release date
1.1	**Documentation**	Nov 14	Nov 26	9d				
1.1.1	wiki	Nov 14	Nov 19	4d		100%		Sat 15 Nov 2008, 22:57: requested hosted.fp
1.1.2	Promotional materials	Nov 20	Nov 26	5d		100%		Update FEL 8-Slides flyer to 10 slides. Get it in time for Mirlan presentation on the 29th - Kyrgyzstan Review and give Aanjhan materials for Foss.in
1.2	**Development**	Nov 3	Nov 18	10d				
1.2.1	**Updating**	Nov 3	Nov 17	9d				
1.2.1.1	gspiceui-0.9.65-3	Nov 3	Nov 3	1d		100%		Updates are already committed. Waiting XamierLamien to push this -3 from testing to stable on F-8 and F-9.
1.2.1.2	gEDA suite	Nov 11	Nov 13	3d		100%		Will need a chain-build from Rel-Eng for libgeda.
1.2.1.3	Piklab-0.15.3-2	Nov 11	Nov 11	1d		100%		Patch broken
1.2.1.4	gerbv-2.1.0	Nov 13	Nov 17	3d		100%		
1.2.1.5	LabPlot-1.6.0.3-1	Nov 17	Nov 17	1d		100%		Need to upload liborigin as well.
1.2.2	**Security**	Nov 18	Nov 18	1d				
1.2.2.1	geda-gnetlist	Nov 18	Nov 18	1d		100%		Tue 18 Nov 2008, 23:48: guile is broken under rawhide. Chitlesh filed a bug against it. Once guile's maintainer rebuils it, all geda-* should be rebuild on rawhide. A patch

Done Open Notebook

Fedora Electronic Lab 11 Development Timel 00:59:48 Sat, 7 Feb

FEL Development Methodology

The reason why FEL is so unique

All languages win

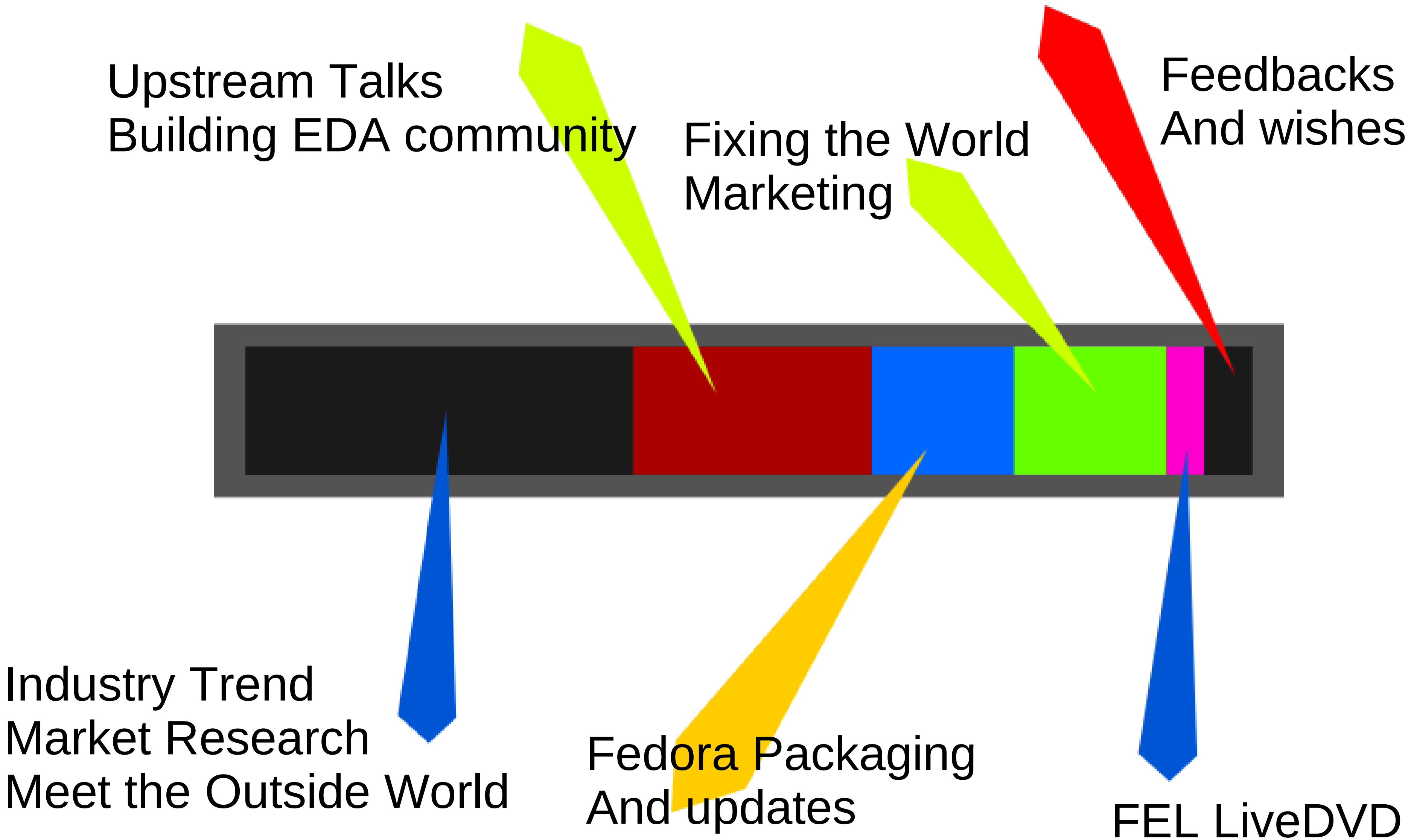
Bottom Up and Top down research Abstraction

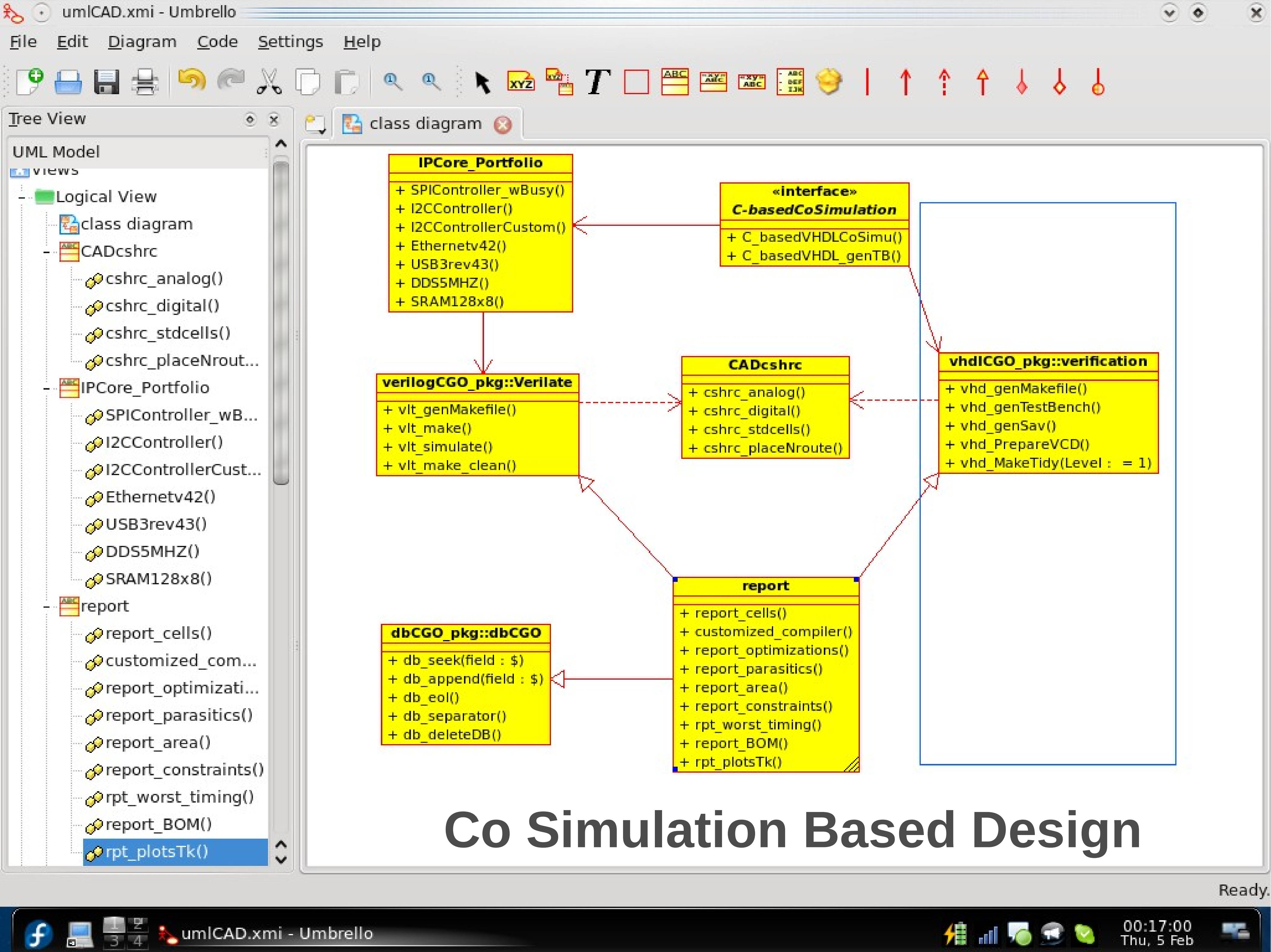
Current Industry Trend

Do not package one's favourite tools only

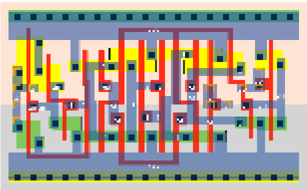
Think Methodology and Design Flow

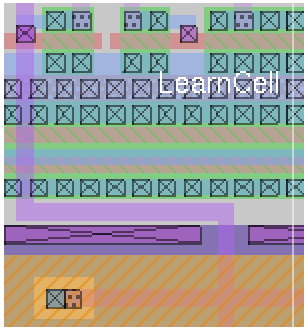
Development Time during One cycle




umlCAD.xmi - Umbrello
File Edit Diagram Code Settings Help
Tree View
UML Model
Views
Logical View
class diagram
CADcshrc
cshrc_analog()
cshrc_digital()
cshrc_stdcells()
cshrc_placeNrout...
IPCore_Portfolio
SPIController_wB...
I2CController()
I2CControllerCust...
Ethernetv42()
USB3rev43()
DDS5MHZ()
SRAM128x8()
report
report_cells()
customized_com...
report_optimizati...
report_parasitics()
report_area()
report_constraints()
rpt_worst_timing()
report_BOM()
rpt_plotsTk()
class diagram
IPCore_Portfolio
+ SPIController_wBusy()
+ I2CController()
+ I2CControllerCustom()
+ Ethernetv42()
+ USB3rev43()
+ DDS5MHZ()
+ SRAM128x8()
«interface»
C-basedCoSimulation
+ C_basedVHDLCoSimu()
+ C_basedVHDL_genTB()
verilogCGO_pkg::Verilate
+ vlt_genMakefile()
+ vlt_make()
+ vlt_simulate()
+ vlt_make_clean()
CADcshrc
+ cshrc_analog()
+ cshrc_digital()
+ cshrc_stdcells()
+ cshrc_placeNroute()
vhdlCGO_pkg::verification
+ vhd_genMakefile()
+ vhd_genTestBench()
+ vhd_genSav()
+ vhd_PrepareVCD()
+ vhd_MakeTidy(Level : = 1)
dbCGO_pkg::dbCGO
+ db_seek(field : $)
+ db_append(field : $)
+ db_eol()
+ db_separator()
+ db_deleteDB()
report
+ report_cells()
+ customized_compiler()
+ report_optimizations()
+ report_parasitics()
+ report_area()
+ report_constraints()
+ rpt_worst_timing()
+ report_BOM()
+ rpt_plotsTk()
Co Simulation Based Design
Ready.
umlCAD.xmi - Umbrello
00:17:00
Thu, 5 Feb

FEL-11 Leonidas





- Perl modules from Veripool
- Hoping gEDA/gaf 1.6
- Ktechlab new release
- C-based synthesis tool verilator
- Centralized location for documentation
- OVM/SystemC dropped

EDAC - Mozilla Firefox
http://edac.org/industry_roadmap.jsp#roadmap
Google

EDA Industry OS Roadmap

(Updated: September 2007)

Guideline for UltraSPARC Solaris		Sun Website
OS Version	OS Vendor General Availability	Earliest Date for Design Starts
Solaris 10	January 2005	Now

Guideline for X86 32-bit Windows		Microsoft Website
OS Version	OS Vendor General Availability	Earliest Date for Design Starts
Windows XP	December 2001	Now
Windows Vista	January 2007	January 2009

Guideline for X86-64 Linux		Redhat & Novell Websites
OS Version	OS Vendor General Availability	Earliest Date for Design Starts
RHEL 4	February 2005	Now
RHEL 5	March 2007	October 2008
SLES 9	August 2004	Now
SLES 10	July 2006	July 2008

EDA CONSORTIUM

Note

- EDA tool suppliers may exceed the Roadmap baselines.
- Future dates are subject to change.
- For comments or questions about the OS roadmap send an email to OSRoadmap@edac.org

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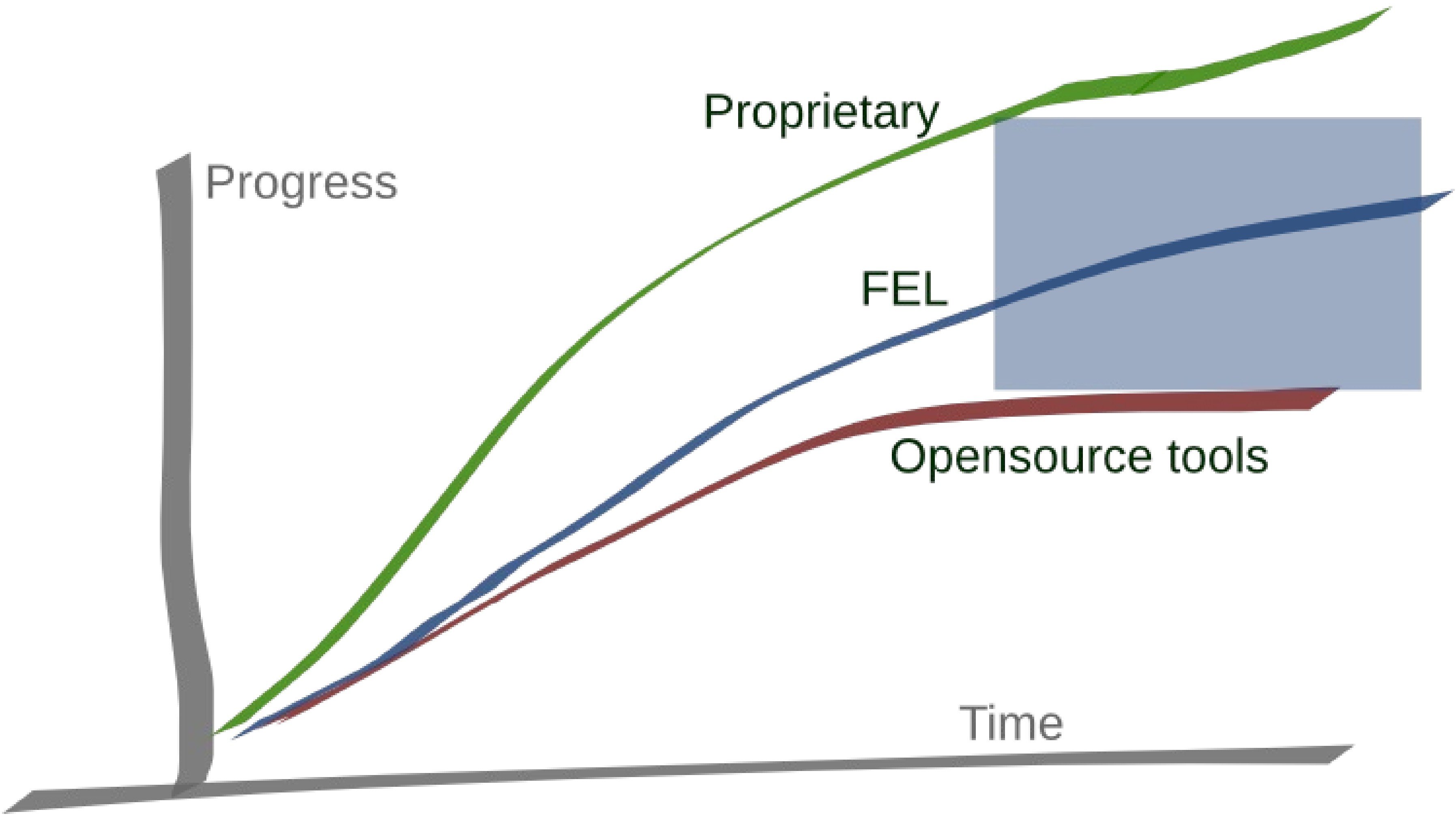
Support Plans of EDA Companies

Done
Open Notebook
EDAC - Mozilla Firefox
00:16:15
Mon, 19 Jan

FEL User and Developer benefits



Long Term goals to achieve

Align FEL along big Vendors in terms of Marketing

Participation in a Standards committee
progress of EDA standards under the IEEE-SA (Standards Association)

Interoperable PDK Libraries

Usage of opensource Industry standard file formats

Strengthen the opensource EDA community

Usage of a common design database

Questions & Answers

The fedora electronic lab team

fedora-electronic-lab-list@redhat.com