



Design, Simulate and Program electronics.

# fedora<sup>TM</sup> *electronic lab*

**Beyond software**

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Fosdem-Brussels  
7-8 February 2009



**Fedora Project**  
has **Man Power** to provide **Open Source Applications** for everything you need.

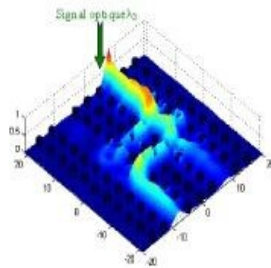
Office

Science/Electronics

Games

Virtualisation /  
Servers

3D Desktop



[ **Quality & Security** ]

[ **Stable & well tested** ]



# [ fedora's Guiding Principles ]

**Encourage Collaborative Development**

**Release Early, Release Often**

**Mutual Benefit of Community and Company**

**Importance of Upstream**



# [ Fedora Electronic Lab ]

**An opensource Design and Simulation platform  
For Electronics**

**A one-stop linux distribution for hardware design**

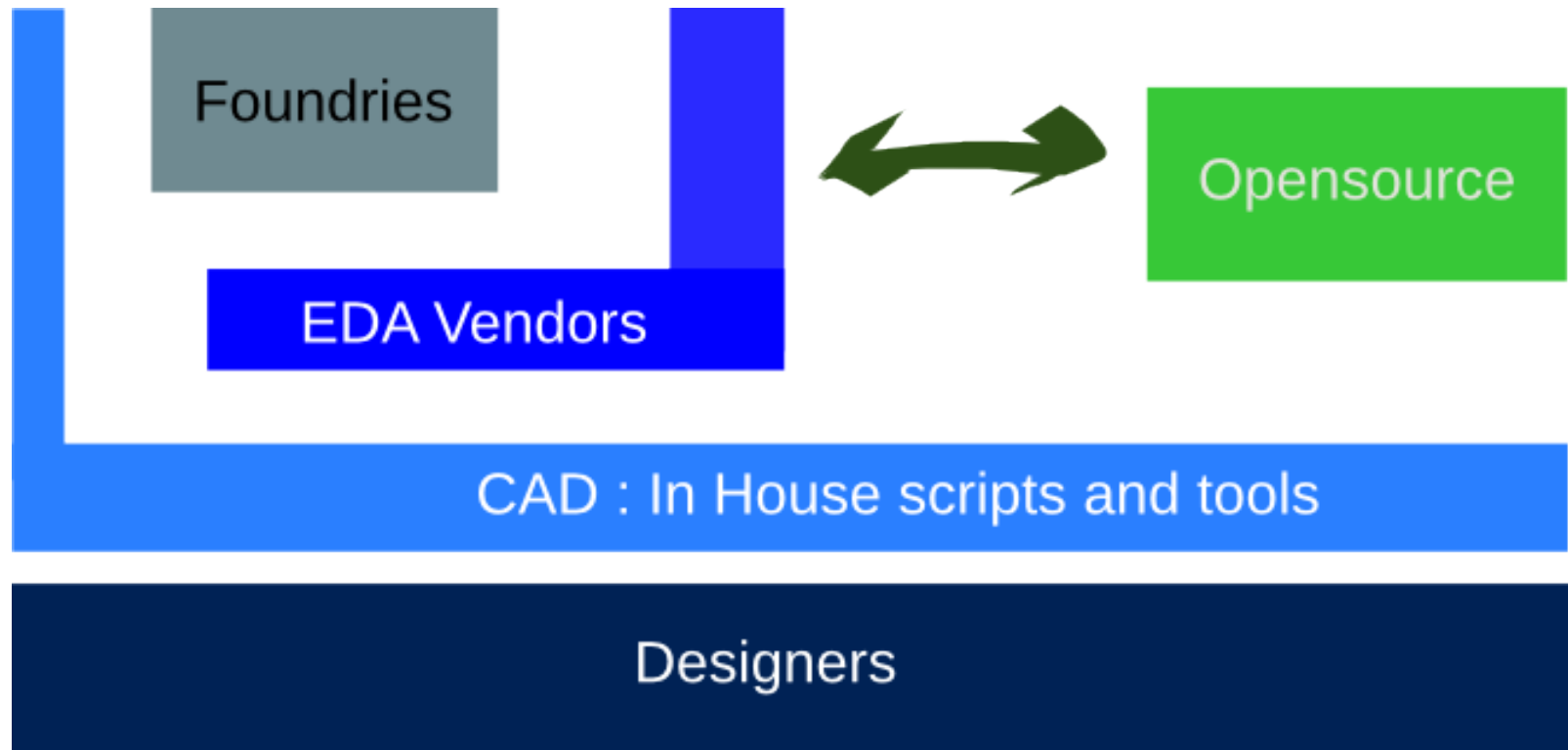
**Marketing means for opensource EDA developers  
(Networking)**



**XUROPA<sup>SM</sup>**



# Identifying a Problem to solve !





# Electronic Designers Problems

Approx. 6 month design development cycle

Tackling Design Complexity

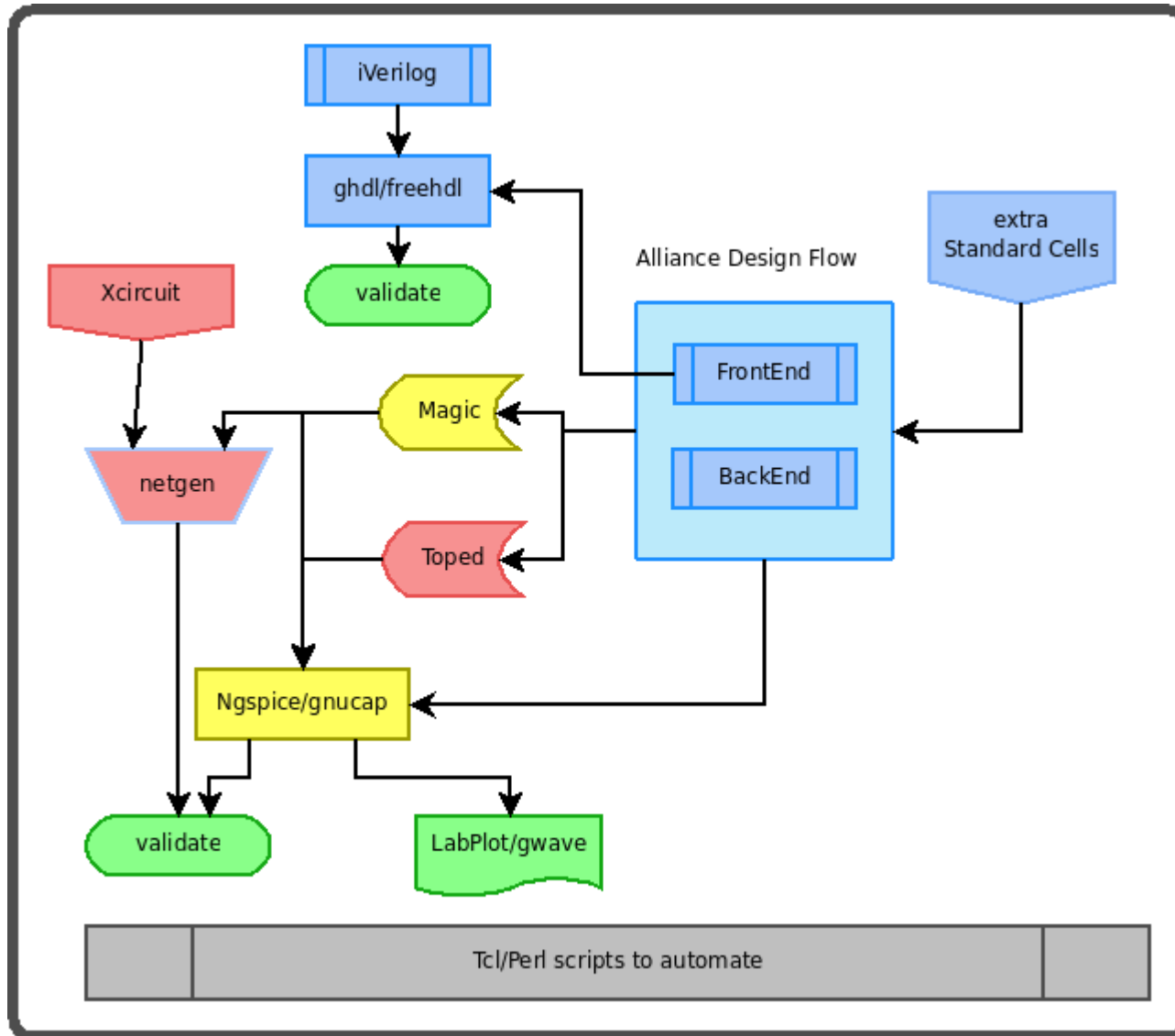
Lower Power, Lower Cost and Smaller Space

EDA Industry's neck squeezed in 2008

Management (digital/analog) IP Portfolio

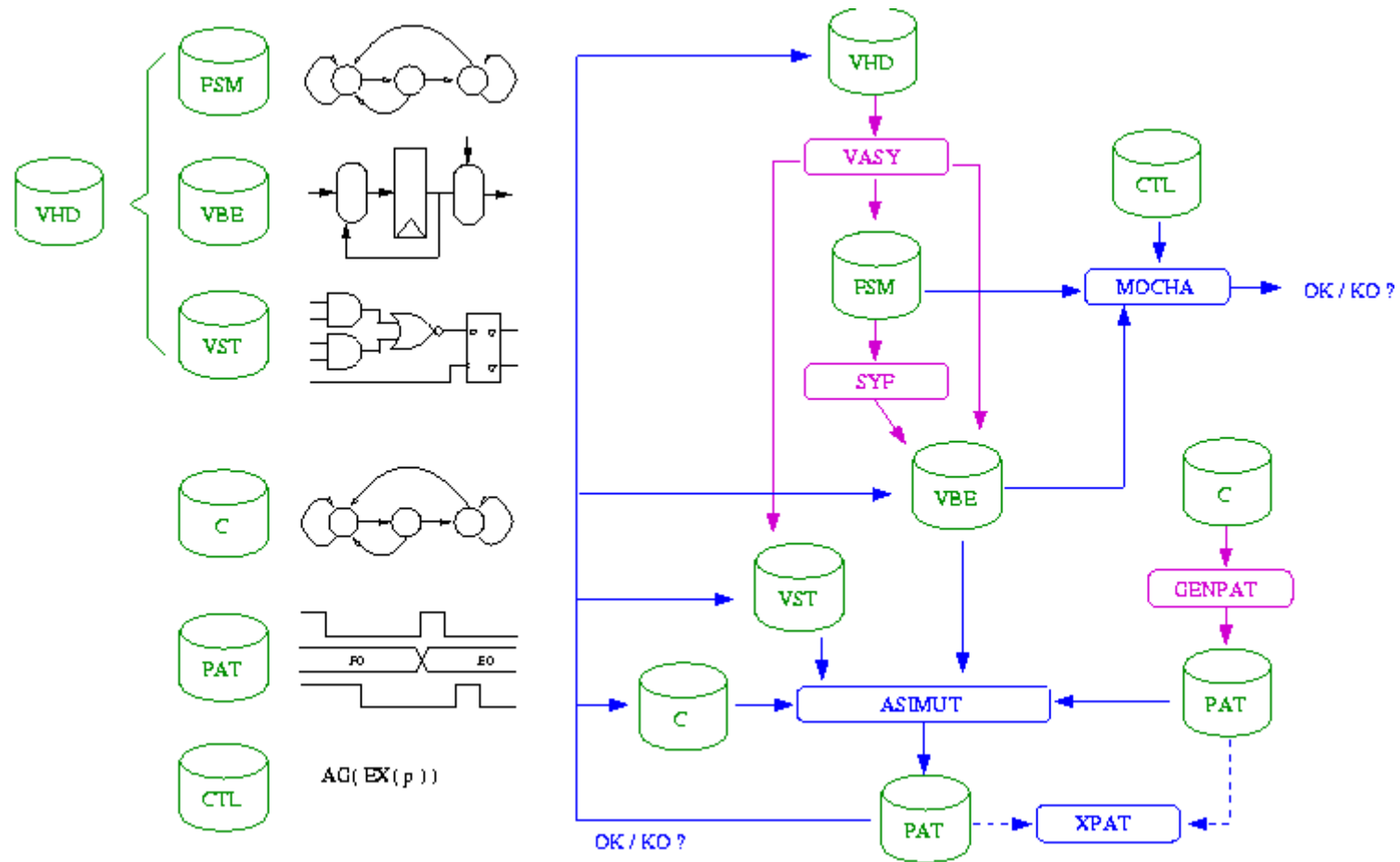


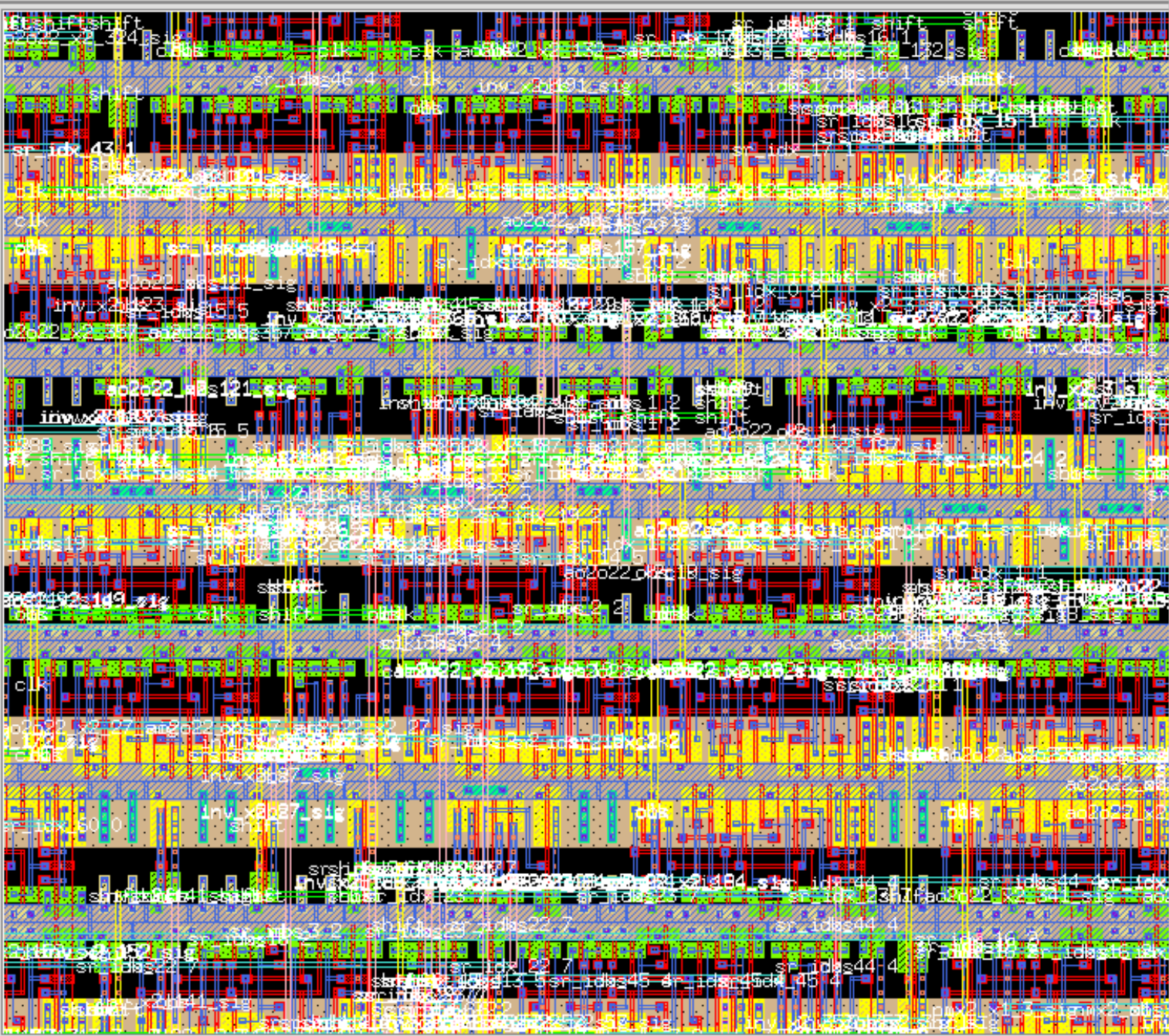
# A basic Design Flow





# Example of RTL Synthesis versus scripting





**Layer**

All visible	All invisible
Nwell	Pwell
Activ	Ndif
Pdif	Ntie
Ptie	Poly
Tpoly	Poly2
Cont	Alu1
VAlu1	Talu1
Via1	TVia1
Alu2	Talu2
Via2	Alu3
Talu3	Via3
Alu4	Talu4
Via4	Alu5
Talu5	Via5
Alu6	Talu6
Ref	Abox
Fig	Inst
FCon	ICon
FSeg	ISeg
FRef	IRef

Pattern Interface  
 Invert Quick display  
 No string box  
 Apply Close

**Arrows <**

← ↑  
 ↓ →

Move Set  
 Close

**Zoom <2**

Refresh  
 UnZoom  
 Zoom  
 Mooz  
 Zoom Set  
 Zoom In  
 Center  
 Goto  
 Pan  
 Fit  
 Close

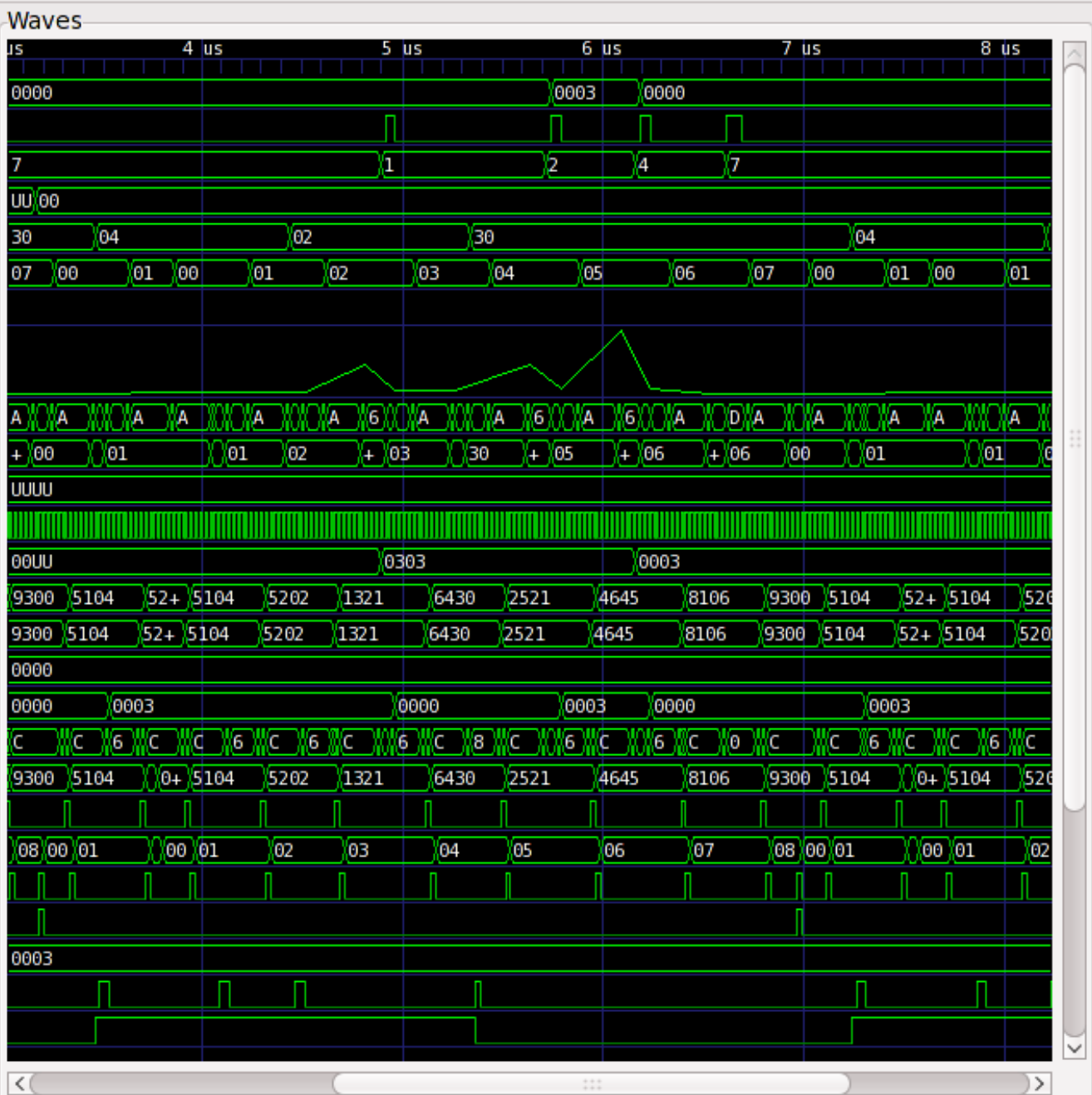
- cpu\_undertest
  - abus\_comp
  - alu\_comp
  - ctrl\_comp
  - dbus\_comp
  - instr\_reg\_comp
  - prog\_counter\_comp
  - ram\_comp
  - register\_file\_comp
  - rom\_comp

- pc\_en
- pc\_ld
- ra\_db[15:0]
- ra\_en
- ra\_rw
- res\_zero
- reset
- ro\_db[15:0]
- rs\_db[15:0]
- rs\_en
- rs\_full
- rs\_rw
- zero

Filter:

Append Insert Replace

- Signals
- Time
- a\_db[15:0] =
  - a\_en =
  - a\_sel[3:0] =
  - ab\_pc[7:0] =
  - ab\_ra[7:0] =
  - ab\_ro[7:0] =
  - ab\_rs[7:0] =
  - ab\_sel[3:0] =
  - cl\_ab[7:0] =
  - cl\_db[15:0] =
  - clk =
  - db\_a[15:0] =
  - db\_cl[15:0] =
  - db\_ir[15:0] =
  - db\_ra[15:0] =
  - db\_rs[15:0] =
  - db\_sel[3:0] =
  - ir\_db[15:0] =
  - ir\_en =
  - pc\_ab[7:0] =
  - pc\_en =
  - pc\_ld =
  - ra\_db[15:0] =
  - ra\_en =
  - ra\_rw =





# How would you shape FEL Development ?



3.3.6.2	Fedora	
3.3.7	<b>Documentation</b>	
3.3.7.1	wiki	
3.3.7.2	promotional materials	
3.3.7.3	hosted repository	
3.3.7.4	aid edu-spin	
3.3.7.5	FOSDEM Flyer	
3.3.7.6	Xuropa Online Booth	
3.3.8	<b>Upstream</b>	
3.3.8.1	geda/gerbv	
3.3.8.2	toped	
3.3.8.3	pcb	
3.3.8.4	verilator vs systemperl	
3.3.8.5	Ktechlab	
3.3.8.6	Promote Opensource EDA commu	
3.3.9	Upstream talks	
3.4	<b>FEL11 Releases</b>	
3.4.1	LiveDVD tuning	
4	FEL12	

**Tasks**

WBS	Name	Start	Finish	Work	Priority	Complete	Cost	Notes
1	<b>FEL10</b>	Nov 3	Nov 26	19d				FEL 10 Cambridge Release date
1.1	<b>Documentation</b>	Nov 14	Nov 26	9d				
1.1.1	wiki	Nov 14	Nov 19	4d		100%		Sat 15 Nov 2008, 22:57: requested hosted.fp
1.1.2	Promotional materials	Nov 20	Nov 26	5d		100%		Update FEL 8-Slides flyer to 10 slides. Get it in time for Mirlan presentation on the 29th - Kyrgyzstan Review and give Aanjhan materials for Foss.in
1.2	<b>Development</b>	Nov 3	Nov 18	10d				
1.2.1	<b>Updating</b>	Nov 3	Nov 17	9d				
1.2.1.1	gspiceui-0.9.65-3	Nov 3	Nov 3	1d		100%		Updates are already committed. Waiting XamierLamien to push this -3 from testing to stable on F-8 and F-9.
1.2.1.2	gEDA suite	Nov 11	Nov 13	3d		100%		Will need a chain-build from Rel-Eng for libgeda.
1.2.1.3	Piklab-0.15.3-2	Nov 11	Nov 11	1d		100%		Patch broken
1.2.1.4	gerbv-2.1.0	Nov 13	Nov 17	3d		100%		
1.2.1.5	LabPlot-1.6.0.3-1	Nov 17	Nov 17	1d		100%		Need to upload liborigin as well.
1.2.2	<b>Security</b>	Nov 18	Nov 18	1d				
1.2.2.1	geda-gnetlist	Nov 18	Nov 18	1d		100%		Tue 18 Nov 2008, 23:48: guile is broken under rawhide. Chitlesh filed a bug against it. Once guile's maintainer rebuilds it, all geda # should be rebuild on rawhide. A patch

Done



# FEL Development Methodology

The reason why FEL is so unique

All languages win

Bottom Up and Top down research Abstraction

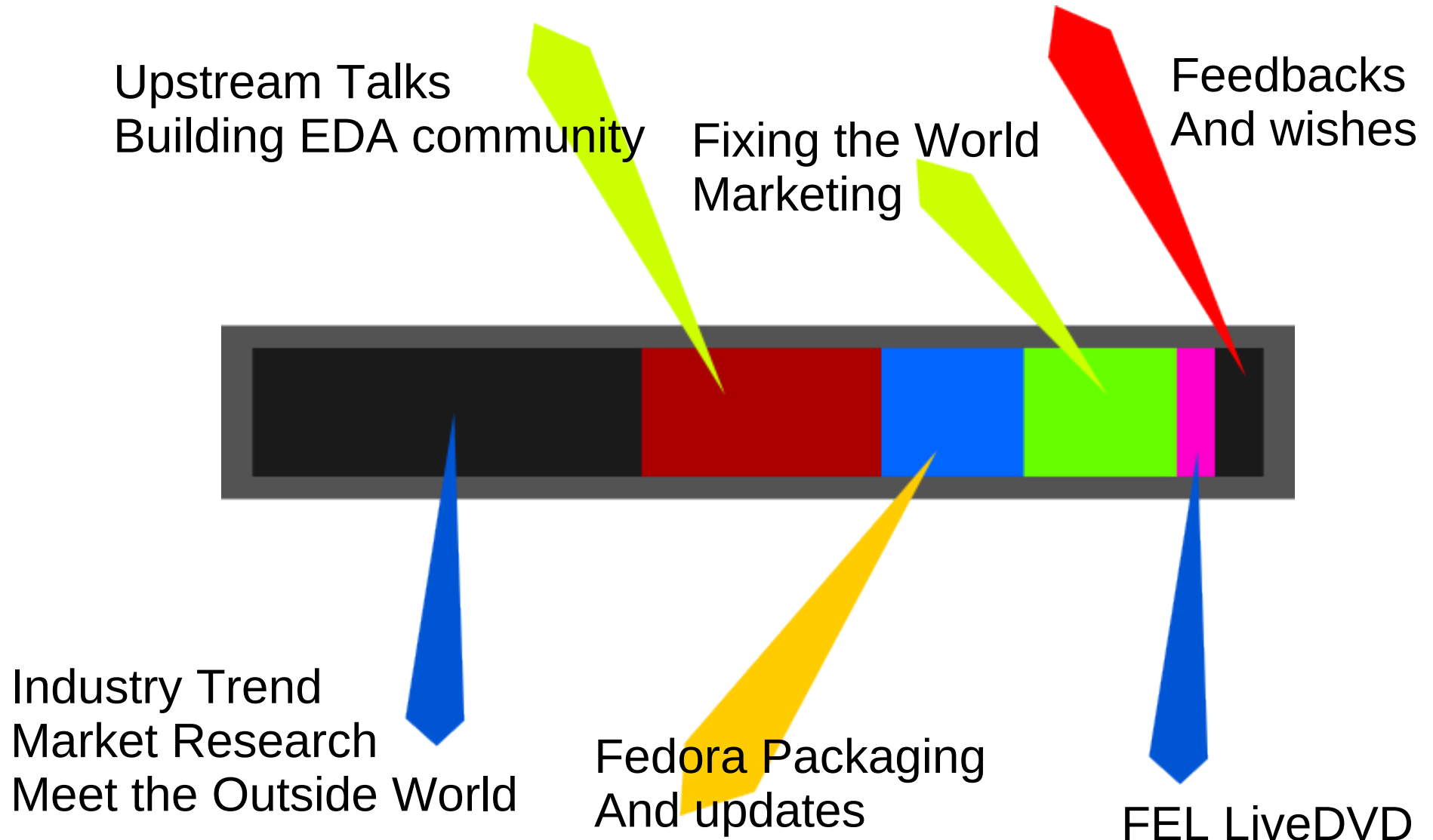
Current Industry Trend

Do not package one's favourite tools only

Think Methodology and Design Flow



# Development Time during One cycle



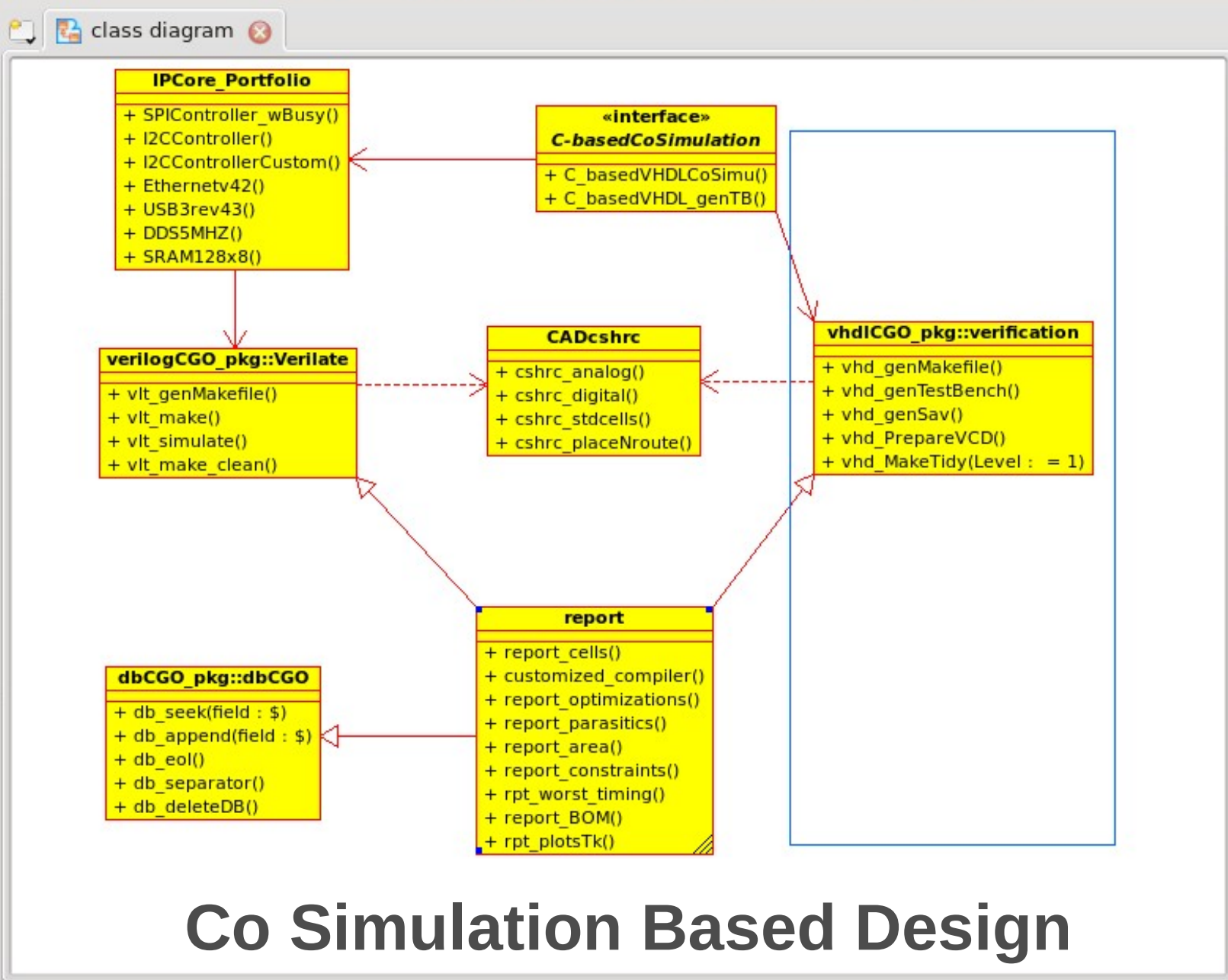


Tree View

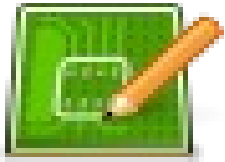
UML Model

views

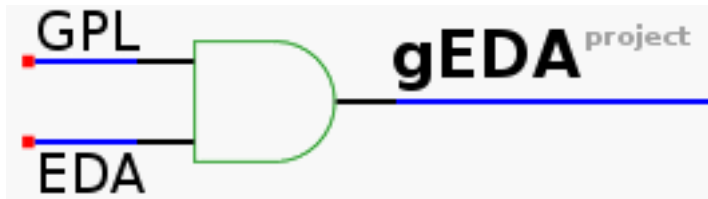
- Logical View
  - class diagram
  - CADcshrc
    - cshrc\_analog()
    - cshrc\_digital()
    - cshrc\_stdcells()
    - cshrc\_placeNroute...
  - IPCore\_Portfolio
    - SPIController\_wB...
    - I2CController()
    - I2CControllerCust...
    - Ethernetv42()
    - USB3rev43()
    - DDS5MHZ()
    - SRAM128x8()
  - report
    - report\_cells()
    - customized\_com...
    - report\_optimizati...
    - report\_parasitics()
    - report\_area()
    - report\_constraints()
    - rpt\_worst\_timing()
    - report\_BOM()
    - rpt\_plotsTk()



# Co Simulation Based Design



# FEL-11 Leonidas



Perl modules from Veripool

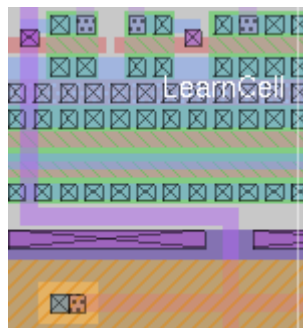
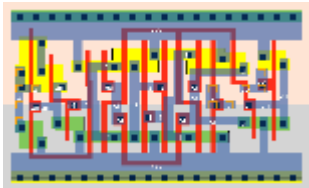
Hoping gEDA/gaf 1.6

Ktechlab new release

C-based synthesis tool verilator

Centralized location for documentation

OVM/SystemC dropped



## EDA Industry OS Roadmap

(Updated: September 2007)

Guideline for UltraSPARC Solaris		<a href="#">Sun Website</a>
OS Version	OS Vendor General Availability	Earliest Date for Design Starts
Solaris 10	January 2005	Now

Guideline for X86 32-bit Windows		<a href="#">Microsoft Website</a>
OS Version	OS Vendor General Availability	Earliest Date for Design Starts
Windows XP	December 2001	Now
Windows Vista	January 2007	January 2009

Guideline for X86-64 Linux		<a href="#">Redhat &amp; Novell Websites</a>
OS Version	OS Vendor General Availability	Earliest Date for Design Starts
RHEL 4	February 2005	Now
RHEL 5	March 2007	October 2008
SLES 9	August 2004	Now
SLES 10	July 2006	July 2008

### Note

- EDA tool suppliers may exceed the Roadmap baselines.
- Future dates are subject to change.
- For comments or questions about the OS roadmap send an email to [OSRoadmap@edac.org](mailto:OSRoadmap@edac.org)

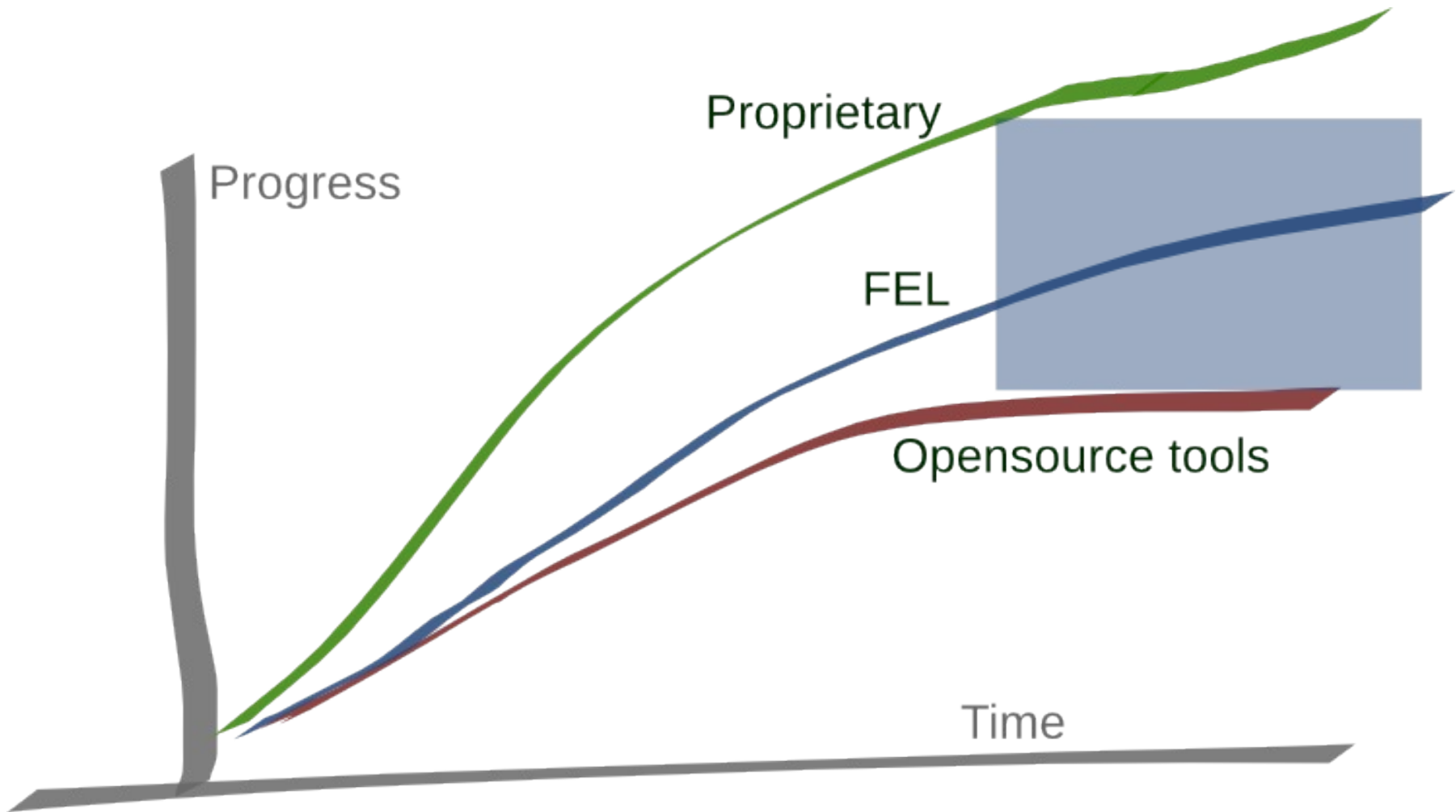
[Back to Top](#)

## Support Plans of EDA Companies





# FEL User and Developer benefits





## Long Term goals to achieve

Align FEL along big Vendors in terms of Marketing

Participation in a Standards committee

progress of EDA standards under the IEEE-SA (Standards Association)

Interoperable PDK Libraries

Usage of opensource Industry standard file formats

Strengthen the opensource EDA community

Usage of a common design database

# Questions & Answers



The **fedora**<sup>™</sup>  **electronic lab team**

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