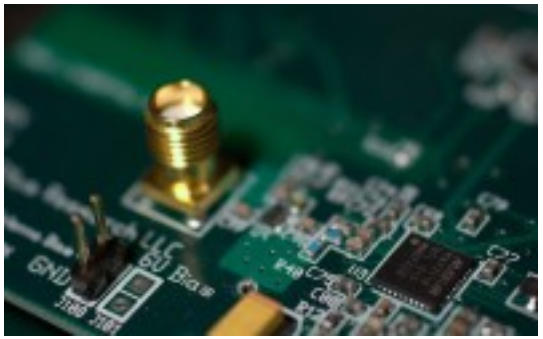
Design, Simulate and Program electronics.

fedora electronic lab

Beyond software

Max Spevack
spevack@fedoraproject.org

FUDCon Berlin
Linuxtag 2009



[Fedora Electronic Lab]

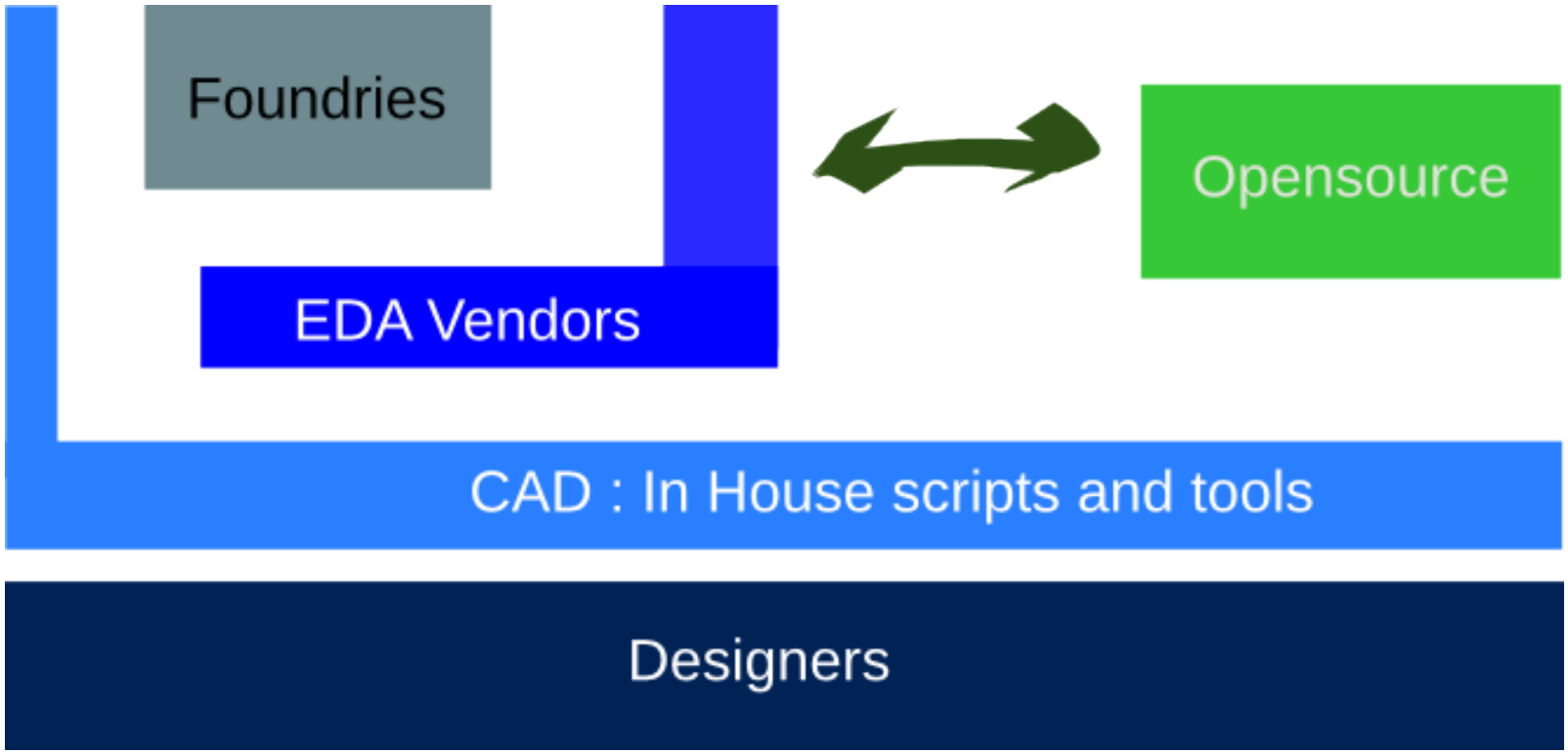
An opensource Design and Simulation platform For Micro-Electronics

A one-stop linux distribution for hardware design

Marketing means for opensource EDA developers (Networking)

XUROPA℠

Identifying a Problem to solve !



Electronic Designers Problems

Approx. 6 month design development cycle

Tackling Design Complexity

Lower Power, Lower Cost and Smaller Space

EDA Industry's neck squeezed in 2008

Management (digital/analog) IP Portfolio

OVERVIEW : FEL'S SOLUTIONS TO THE DESIGN CENTER

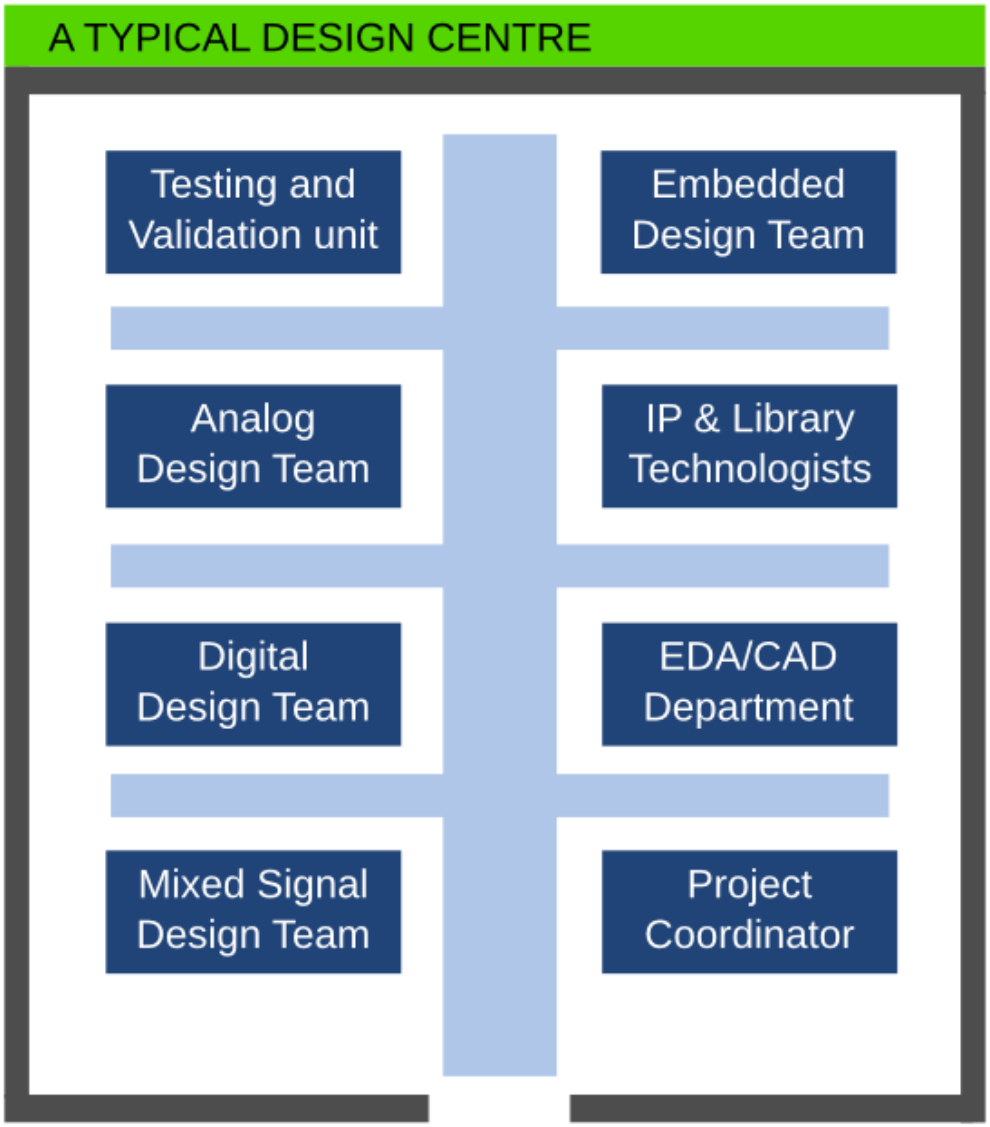
Providing EDA solutions for the real world requires a clear overview on the targetted users.

Fedora Electronic Lab strives to fulfill all the needs of each stage of the design flow .

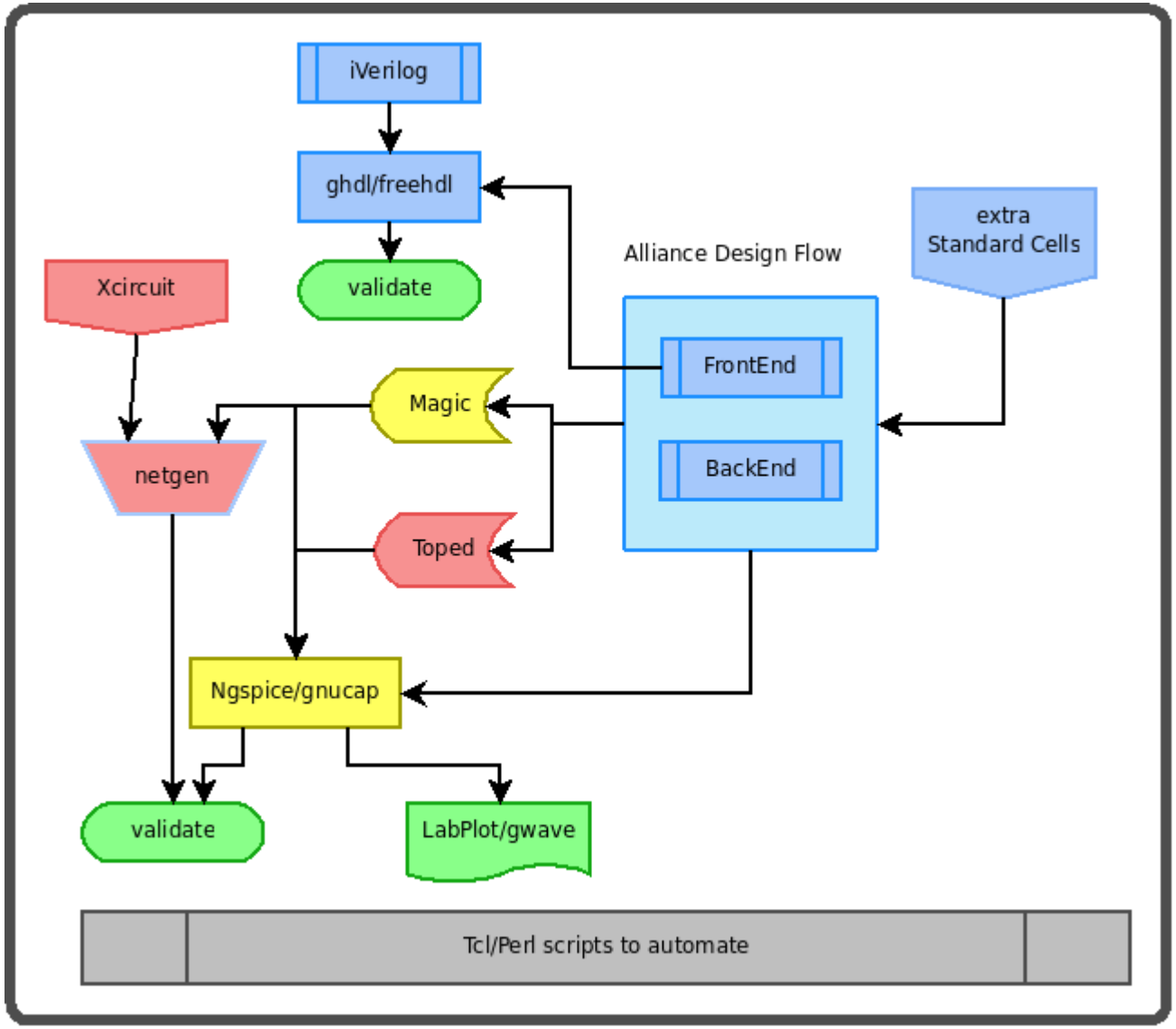
Fedora Electronic Lab

Fedora Electronic Lab improves hardware design experience with opensource software.

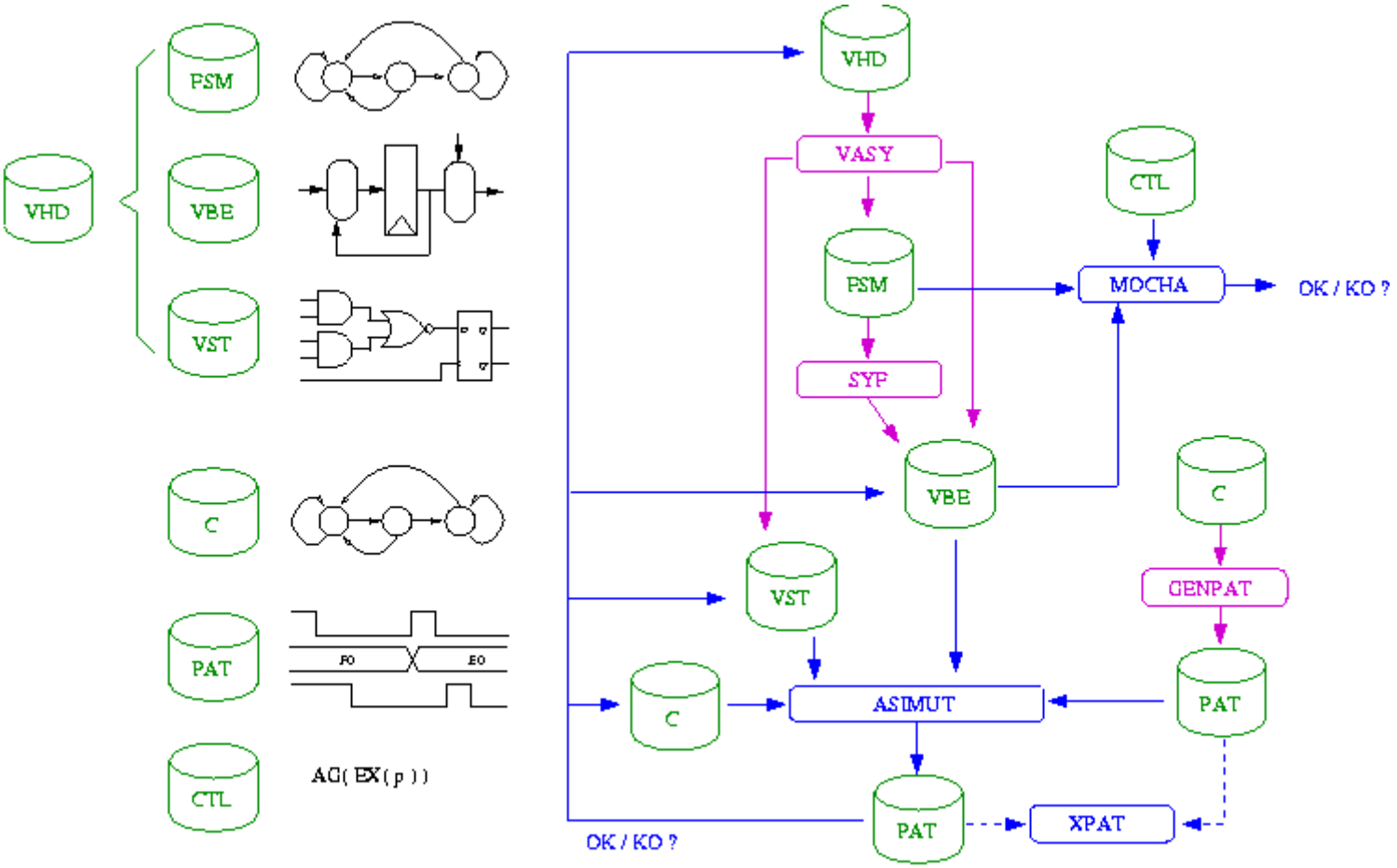
http://chitlesh.fedorapeople.org/FEL

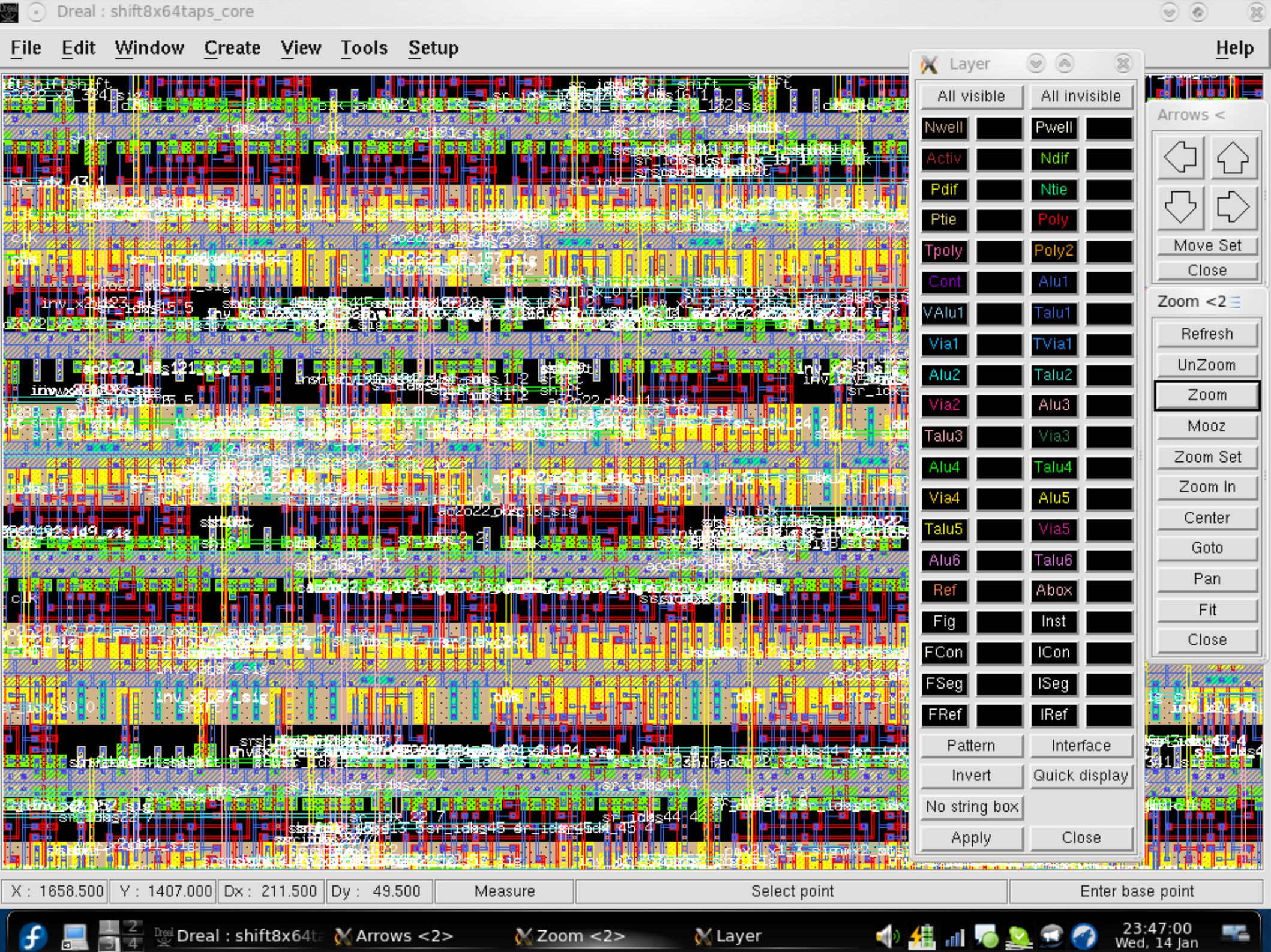


A basic Design Flow



Example of RTL Synthesis versus scripting




Dreal : shift8x64taps_core
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Window
Create
View
Tools
Setup
Help
Layer
All visible
All invisible
Nwell
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Ndif
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Abox
Fig
Inst
FCon
ICon
FSeg
ISeg
FRef
IRef
Pattern
Interface
Invert
Quick display
No string box
Apply
Close
Arrows <
Move Set
Close
Zoom <2
Refresh
UnZoom
Zoom
Mooz
Zoom Set
Zoom In
Center
Goto
Pan
Fit
Close
X : 1658.500
Y : 1407.000
Dx : 211.500
Dy : 49.500
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Select point
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Arrows <2>
Zoom <2>
Layer
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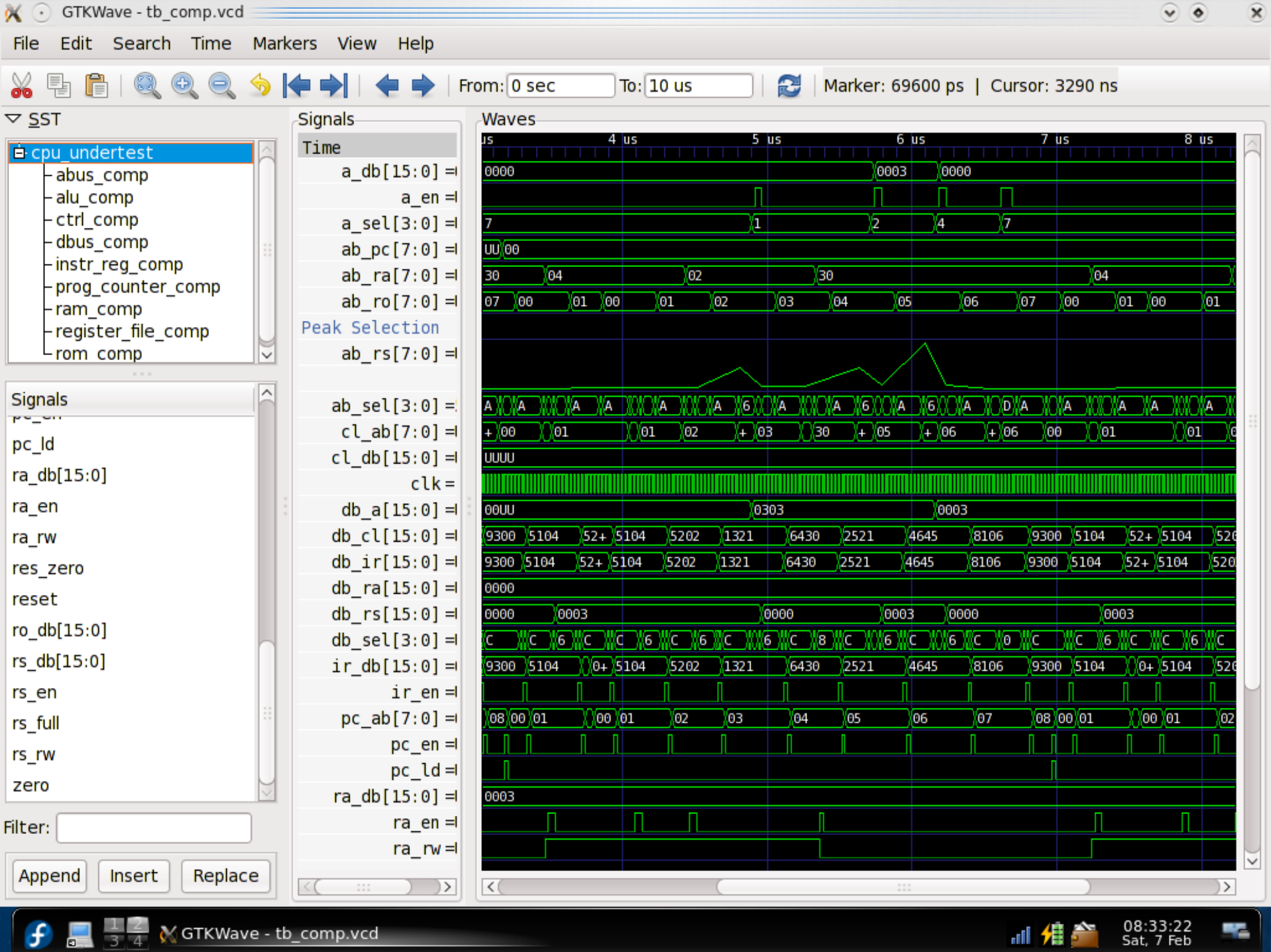
Wed, 14 Jan


GTKWave - tb_comp.vcd
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From: 0 sec
To: 10 us
Marker: 69600 ps | Cursor: 3290 ns
SST
cpu_undertest
abus_comp
alu_comp
ctrl_comp
dbus_comp
instr_reg_comp
prog_counter_comp
ram_comp
register_file_comp
rom_comp
Signals
pc_ld
ra_db[15:0]
ra_en
ra_rw
res_zero
reset
ro_db[15:0]
rs_db[15:0]
rs_en
rs_full
rs_rw
zero
Filter:
Append
Insert
Replace
Signals
Time
a_db[15:0]
a_en
a_sel[3:0]
ab_pc[7:0]
ab_ra[7:0]
ab_ro[7:0]
Peak Selection
ab_rs[7:0]
ab_sel[3:0]
cl_ab[7:0]
cl_db[15:0]
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db_a[15:0]
db_cl[15:0]
db_ir[15:0]
db_ra[15:0]
db_rs[15:0]
db_sel[3:0]
ir_db[15:0]
ir_en
pc_ab[7:0]
pc_en
pc_ld
ra_db[15:0]
ra_en
ra_rw
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4 us
5 us
6 us
7 us
8 us
GTKWave - tb_comp.vcd
08:33:22
Sat, 7 Feb

OVERVIEW : FEDORA'S HIGH END HARDWARE DESIGN PLATFORM

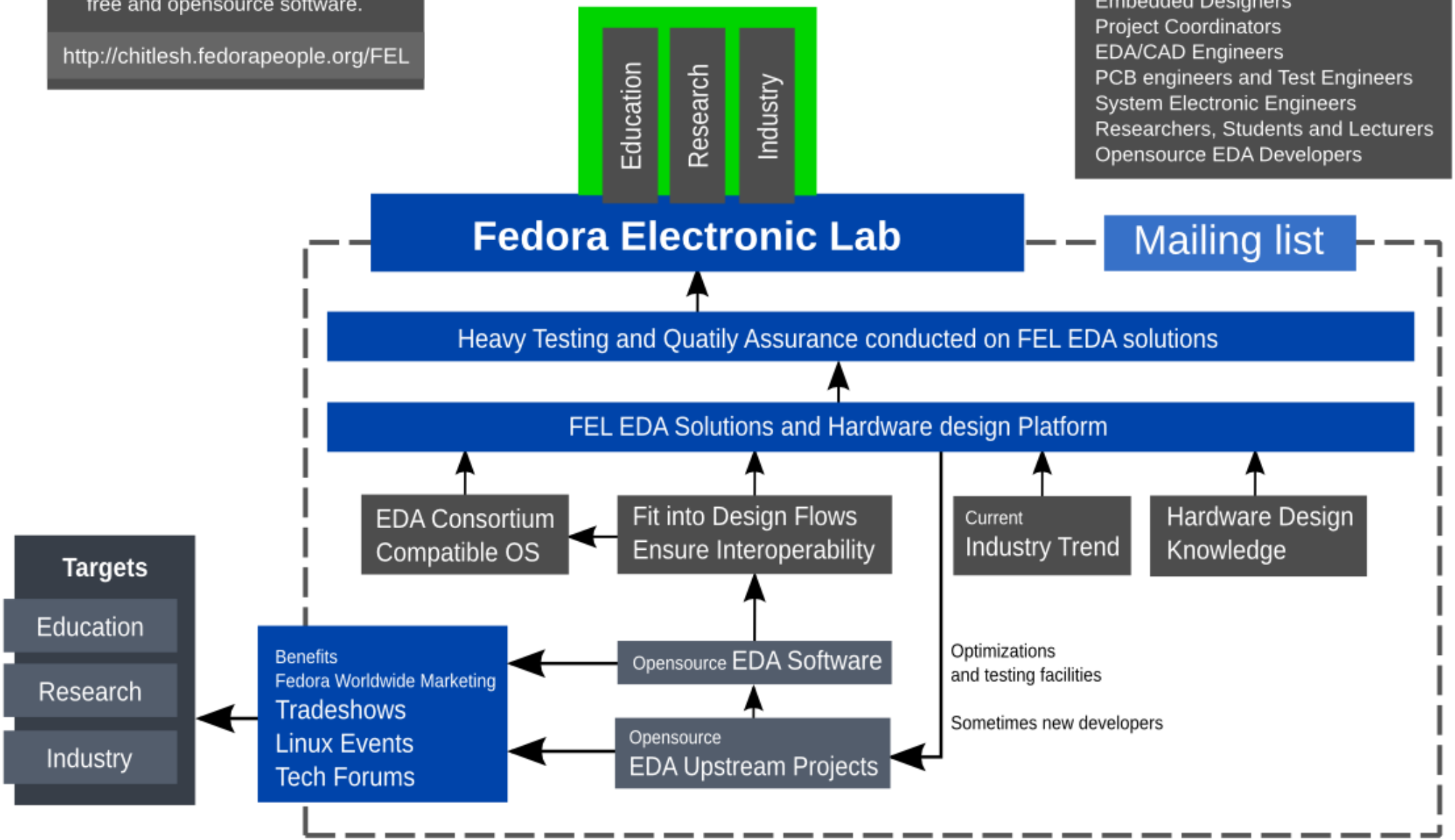
Fedora Electronic Lab

Fedora Electronic Lab improves hardware design experience with free and opensource software.

http://chitlesh.fedorapeople.org/FEL

Benefits

Analog/Digital/Mixed Designers
Verification solutions
Embedded Designers
Project Coordinators
EDA/CAD Engineers
PCB engineers and Test Engineers
System Electronic Engineers
Researchers, Students and Lecturers
Opensource EDA Developers



FEL Development Methodology

The reason why FEL is so unique

All languages win

Bottom Up and Top down research Abstraction

Current Industry Trend

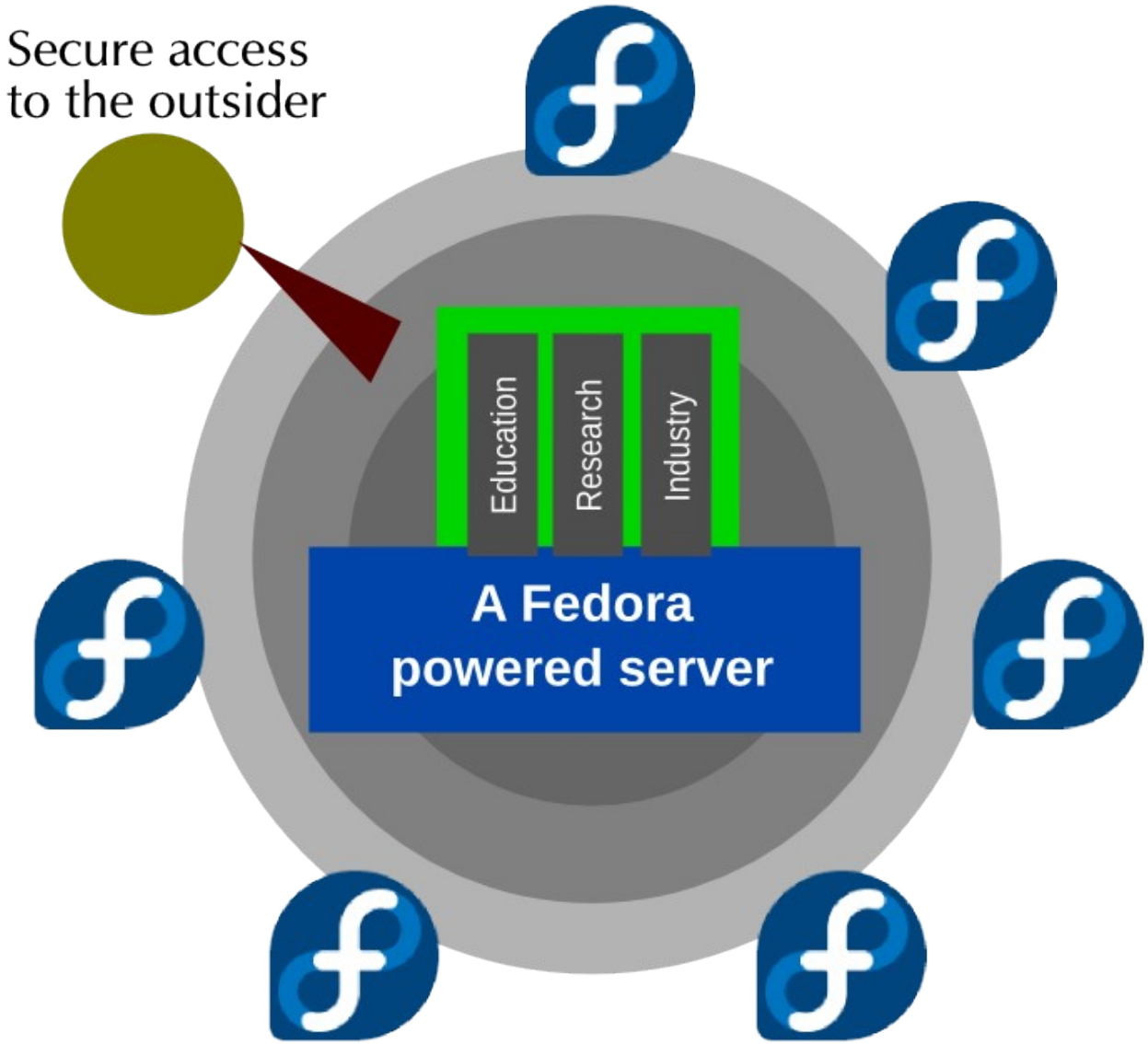
Do not package one's favourite tools only

Think Methodology and Design Flow

Development Time during One cycle

Fedora : Collaborative hardware development

Fedora Electronic Lab



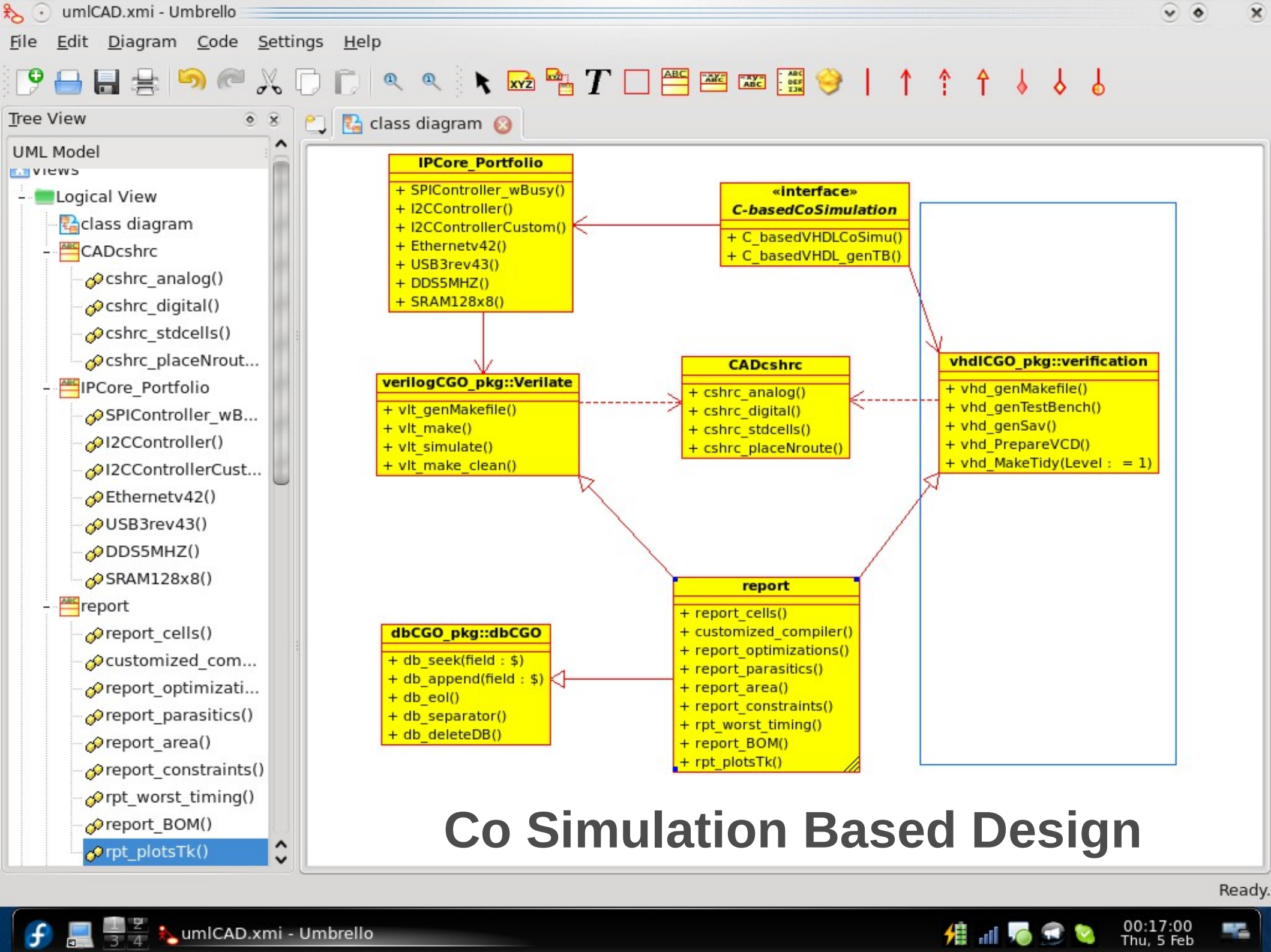
http://chitlesh.fedorapeople.org/FEL

Deployment of a simple Code Review Solution for
- digital IC design
- FPGA design
- embedded design

A Fedora powered server hosting a wiki, web-based version control, progress tracking feature, ticketing service and peer review feature.

Fedora desktops with electronic design and simulation tools coupled with Fedora Eclipse and its plugins.

From Fedora Eclipse, easy and simple HDL code management along with code review via a browser.


umlCAD.xmi - Umbrello
File Edit Diagram Code Settings Help
Tree View
UML Model
Logical View
class diagram
CADcshrc
cshrc_analog()
cshrc_digital()
cshrc_stdcells()
cshrc_placeNrout...
IPCore_Portfolio
SPIController_wB...
I2CController()
I2CControllerCust...
Ethernetv42()
USB3rev43()
DDS5MHZ()
SRAM128x8()
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report_cells()
customized_com...
report_optimizati...
report_parasitics()
report_area()
report_constraints()
rpt_worst_timing()
report_BOM()
rpt_plotsTk()
class diagram
IPCore_Portfolio
+ SPIController_wBusy()
+ I2CController()
+ I2CControllerCustom()
+ Ethernetv42()
+ USB3rev43()
+ DDS5MHZ()
+ SRAM128x8()
«interface»
C-basedCoSimulation
+ C_basedVHDLCoSimu()
+ C_basedVHDL_genTB()
verilogCGO_pkg::Verilate
+ vlt_genMakefile()
+ vlt_make()
+ vlt_simulate()
+ vlt_make_clean()
CADcshrc
+ cshrc_analog()
+ cshrc_digital()
+ cshrc_stdcells()
+ cshrc_placeNroute()
vhdlCGO_pkg::verification
+ vhd_genMakefile()
+ vhd_genTestBench()
+ vhd_genSav()
+ vhd_PrepareVCD()
+ vhd_MakeTidy(Level : = 1)
report
+ report_cells()
+ customized_compiler()
+ report_optimizations()
+ report_parasitics()
+ report_area()
+ report_constraints()
+ rpt_worst_timing()
+ report_BOM()
+ rpt_plotsTk()
dbCGO_pkg::dbCGO
+ db_seek(field : $)
+ db_append(field : $)
+ db_eol()
+ db_separator()
+ db_deleteDB()
Co Simulation Based Design
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umlCAD.xmi - Umbrello
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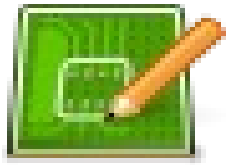
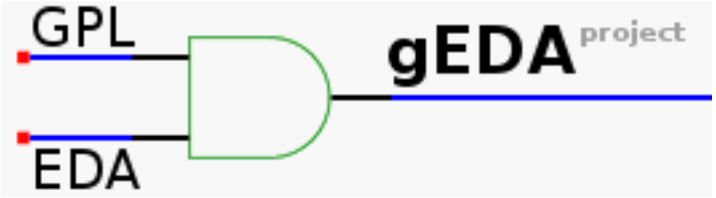
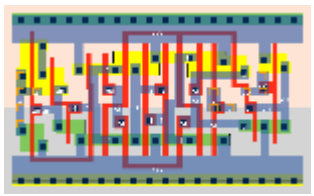
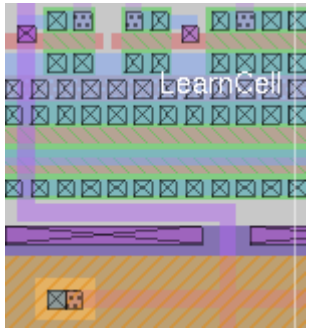
Thu, 5 Feb



FEL-11 Leonidas







Perl modules from Veripool

Hoping gEDA/gaf 1.6

Ktechlab new release

C-based synthesis tool verilator

Centralized location for documentation

OVM/SystemC dropped

EDA Industry OS Roadmap

(Updated: September 2007)

Guideline for UltraSPARC Solaris		Sun Website
OS Version	**OS Vendor General Availability**	**Earliest Date for Design Starts**
Solaris 10	January 2005	Now

Guideline for X86 32-bit Windows		Microsoft Website
OS Version	**OS Vendor General Availability**	**Earliest Date for Design Starts**
Windows XP	December 2001	Now
Windows Vista	January 2007	January 2009

Guideline for X86-64 Linux		Redhat & Novell Websites
OS Version	**OS Vendor General Availability**	**Earliest Date for Design Starts**
RHEL 4	February 2005	Now
RHEL 5	March 2007	October 2008
SLES 9	August 2004	Now
SLES 10	July 2006	July 2008

Note

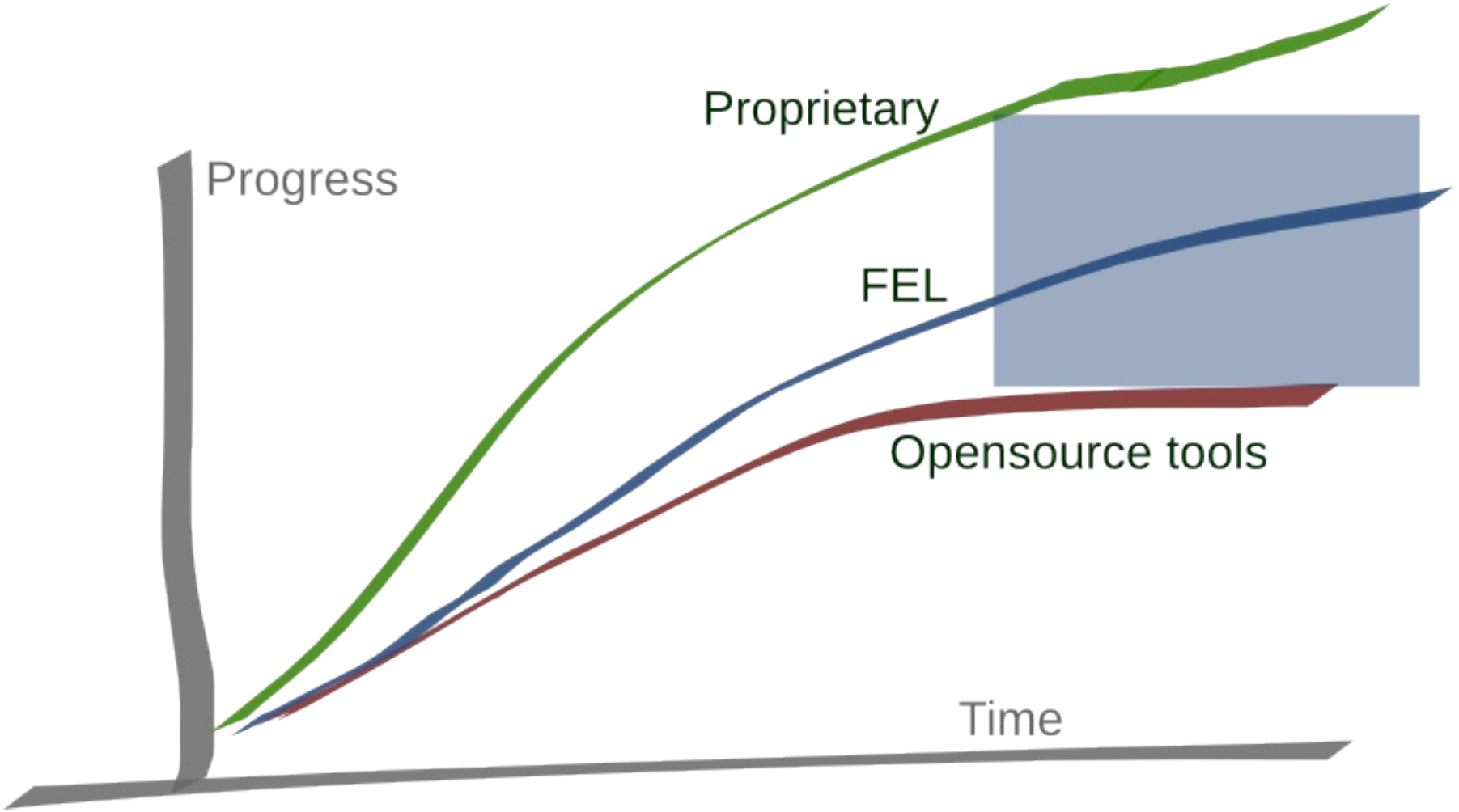
- EDA tool suppliers may exceed the Roadmap baselines.
- Future dates are subject to change.
- For comments or questions about the OS roadmap send an email to OSRoadmap@edac.org

Back to Top

Support Plans of EDA Companies

EDA CONSORTIUM

FEL User and Developer benefits



Long Term goals to achieve

Align FEL along big Vendors in terms of Marketing

Participation in a Standards committee
progress of EDA standards under the IEEE-SA (Standards Association)

Interoperable PDK Libraries

Usage of opensource Industry standard file formats

Strengthen the opensource EDA community

Usage of a common design database

Questions & Answers


The fedora electronic lab team
fedora-electronic-lab-list@redhat.com