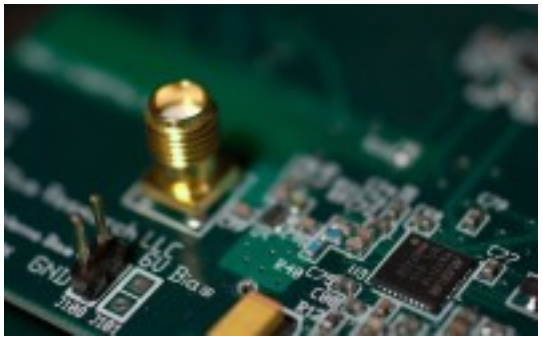
Design, Simulate and Program electronics.

fedora™ *electronic lab*

When software is not enough

Chitlesh Goorah
chitlesh@fedoraproject.org

FUDCon Berlin
Linuxtag 2009



[Fedora Electronic Lab]

An opensource Design and Simulation platform For Micro-Electronics

A one-stop linux distribution for hardware design

Marketing means for opensource EDA developers (Networking)

XUROPA℠

Fedora Electronic Lab 4.0 ?

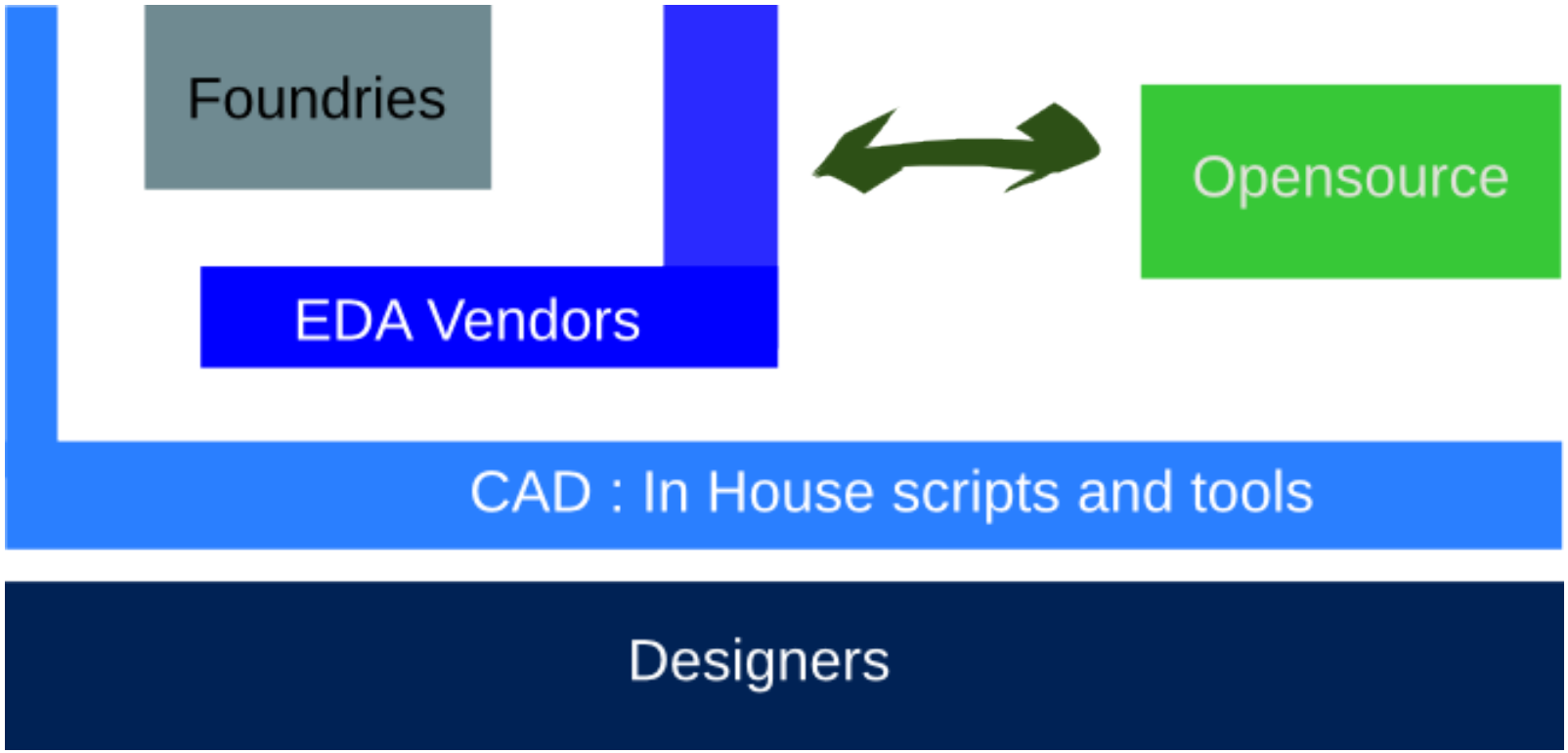
Satisfy User “ME”

Strengthening the Backbone

Ensuring Interchangeability

FrontEnd design experience

Identifying a Problem to solve !



Electronic Designers Problems

Approx. 6 month design development cycle

Tackling Design Complexity

Lower Power, Lower Cost and Smaller Space

EDA Industry's neck squeezed in 2008

Management (digital/analog) IP Portfolio

OVERVIEW : FEL'S SOLUTIONS TO THE DESIGN CENTER

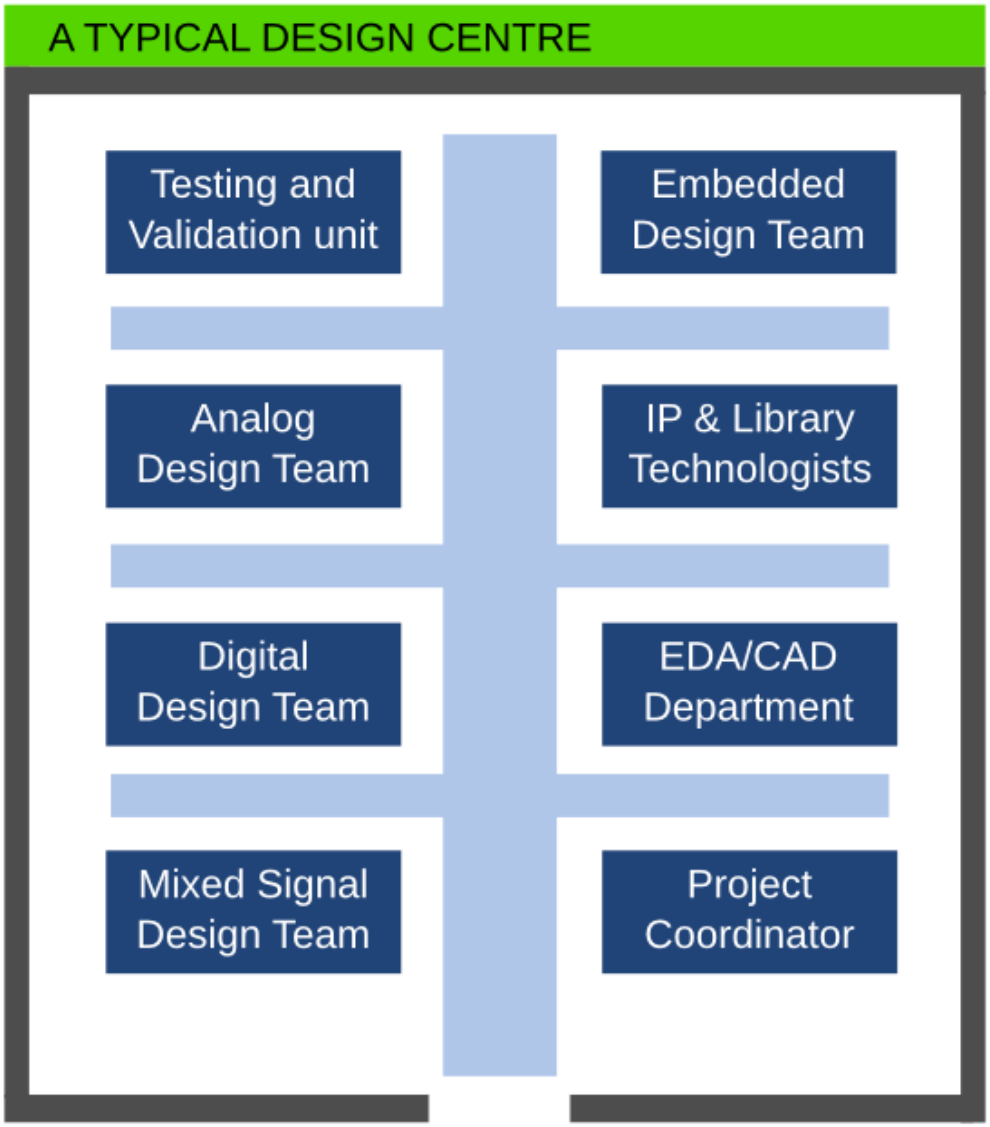
Providing EDA solutions for the real world requires a clear overview on the targetted users.

Fedora Electronic Lab strives to fulfill all the needs of each stage of the design flow .

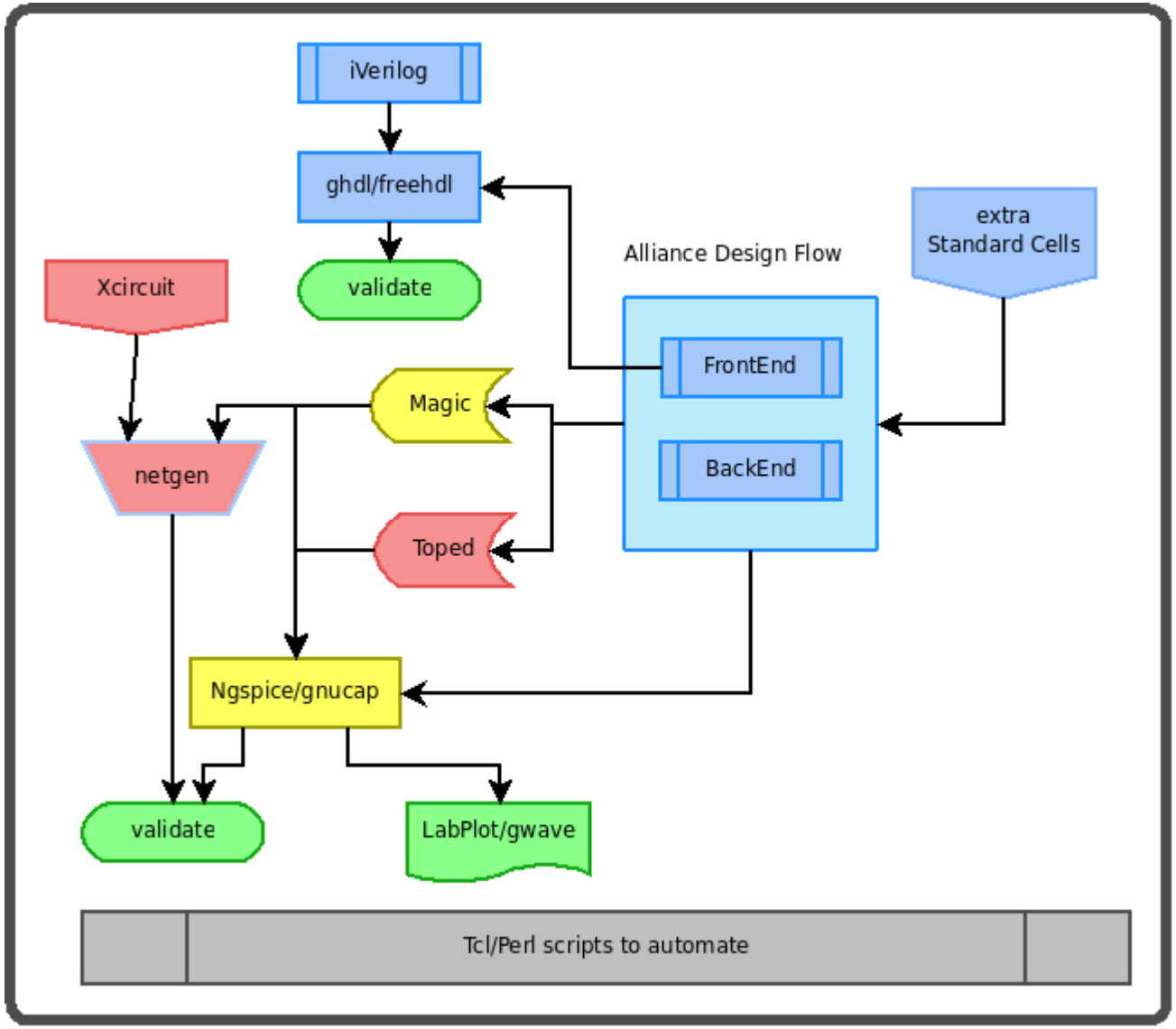
Fedora Electronic Lab

Fedora Electronic Lab improves hardware design experience with opensource software.

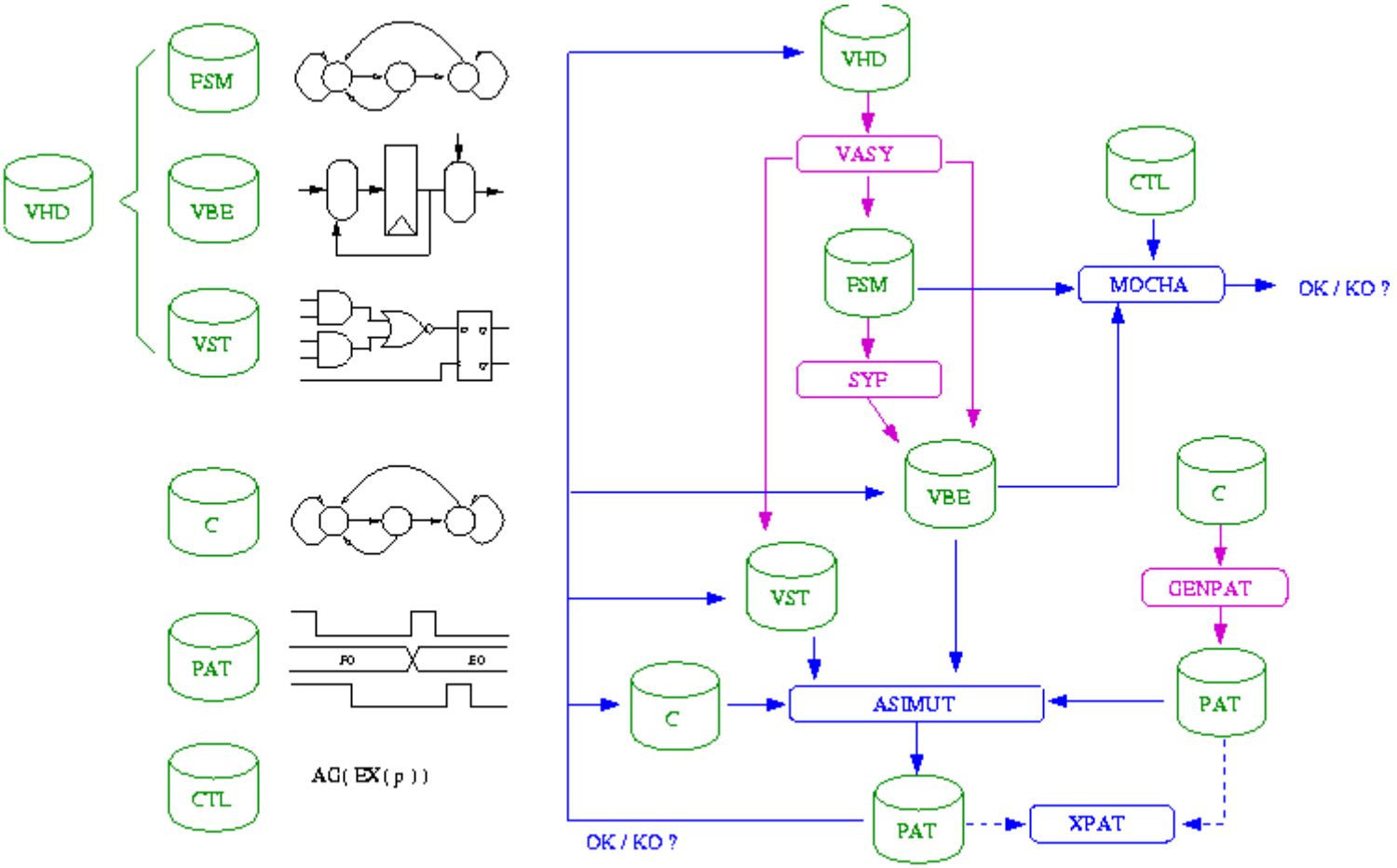
http://chitlesh.fedorapeople.org/FEL

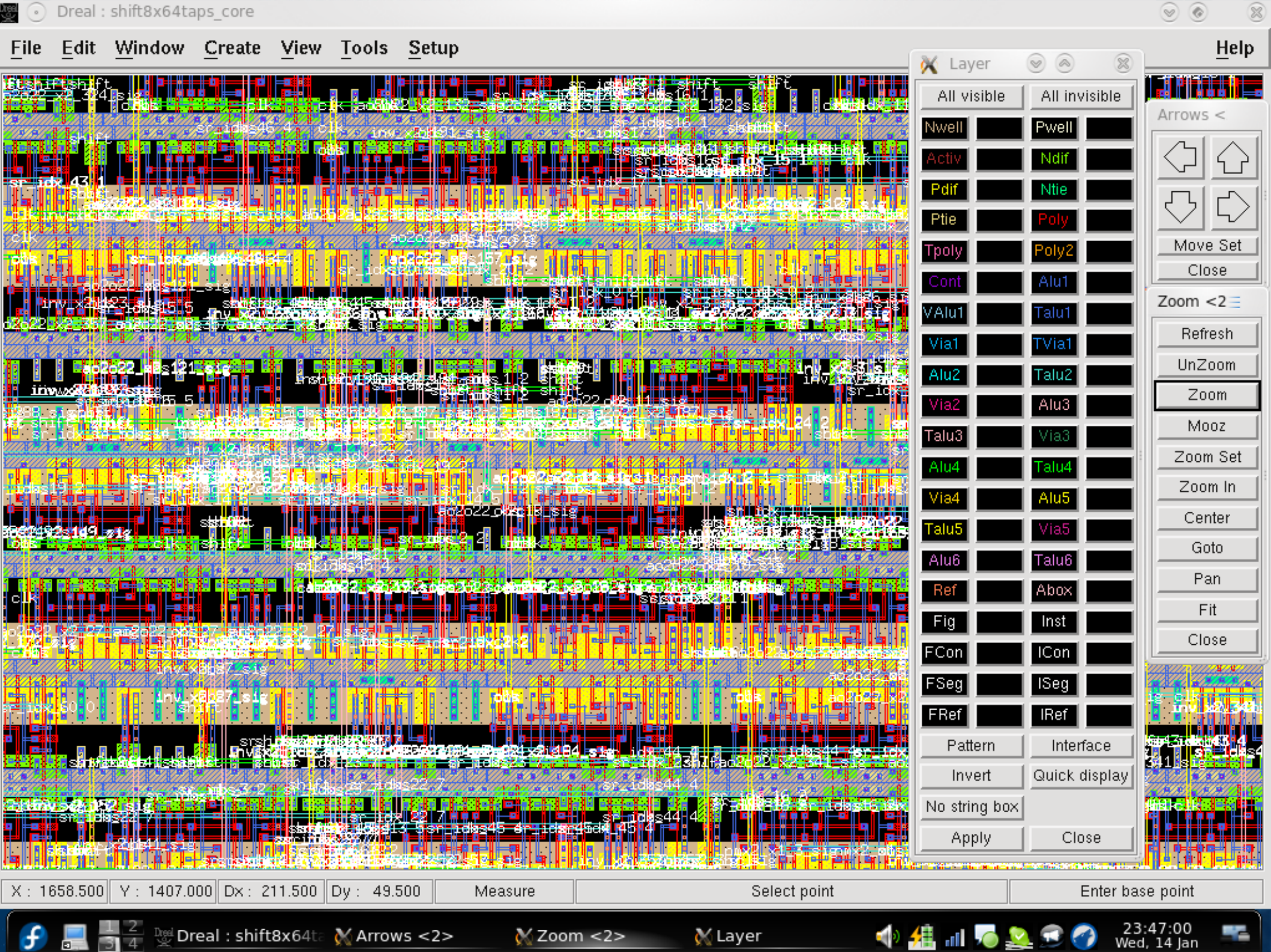


A basic Design Flow



Example of RTL Synthesis versus scripting

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Dy : 49.500
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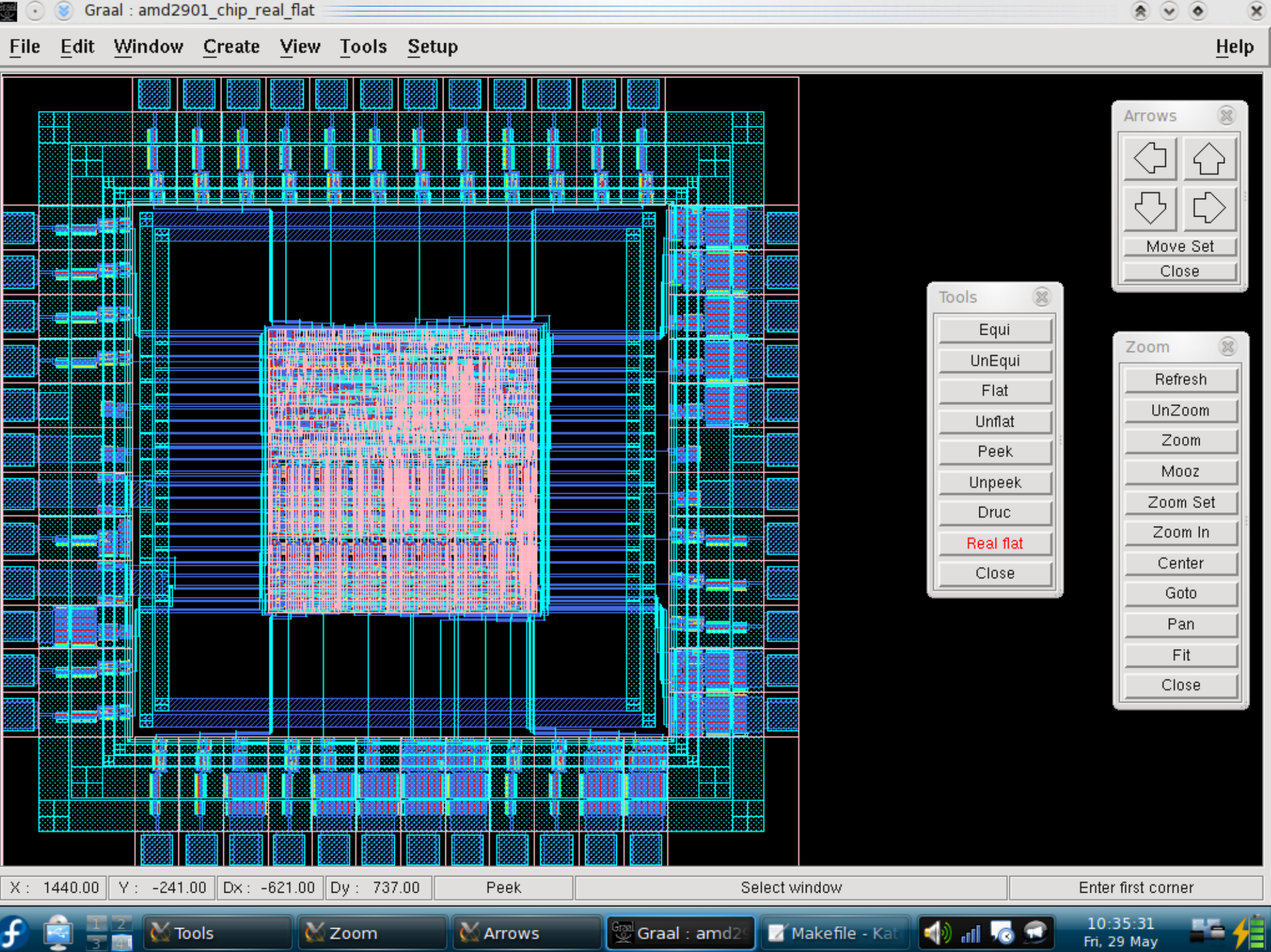
Wed, 14 Jan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Y : -241.00
Dx : -621.00
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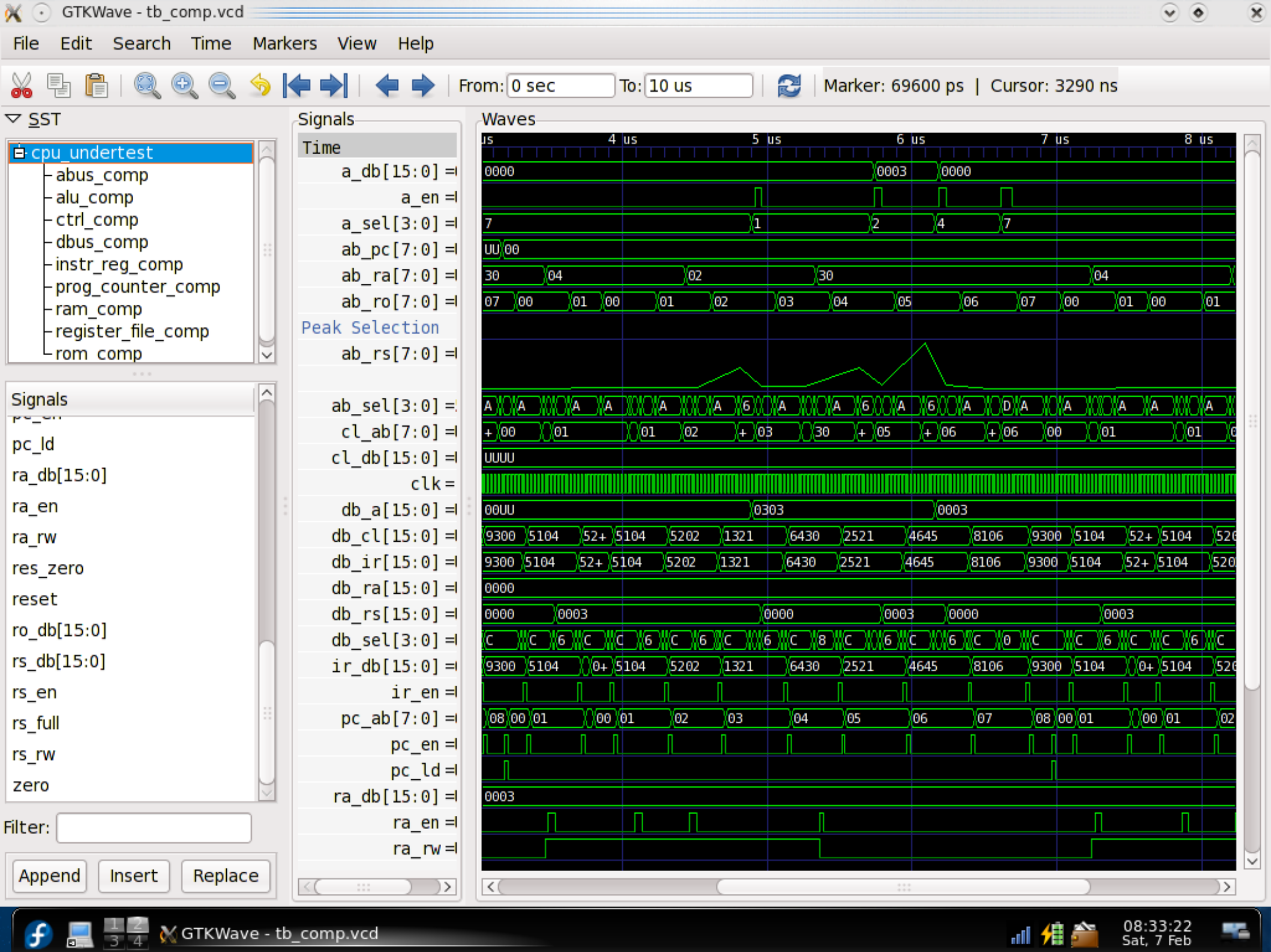
Makefile - Kat
10:35:31
Fri, 29 May


GTKWave - tb_comp.vcd
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From: 0 sec
To: 10 us
Marker: 69600 ps | Cursor: 3290 ns
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cpu_undertest
abus_comp
alu_comp
ctrl_comp
dbus_comp
instr_reg_comp
prog_counter_comp
ram_comp
register_file_comp
rom_comp
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pc_ld
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ra_en
ra_rw
res_zero
reset
ro_db[15:0]
rs_db[15:0]
rs_en
rs_full
rs_rw
zero
Filter:
Append
Insert
Replace
Signals
Time
a_db[15:0]
a_en
a_sel[3:0]
ab_pc[7:0]
ab_ra[7:0]
ab_ro[7:0]
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ab_rs[7:0]
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db_ra[15:0]
db_rs[15:0]
db_sel[3:0]
ir_db[15:0]
ir_en
pc_ab[7:0]
pc_en
pc_ld
ra_db[15:0]
ra_en
ra_rw
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5 us
6 us
7 us
8 us
GTKWave - tb_comp.vcd
08:33:22
Sat, 7 Feb

PCB: temp_collector

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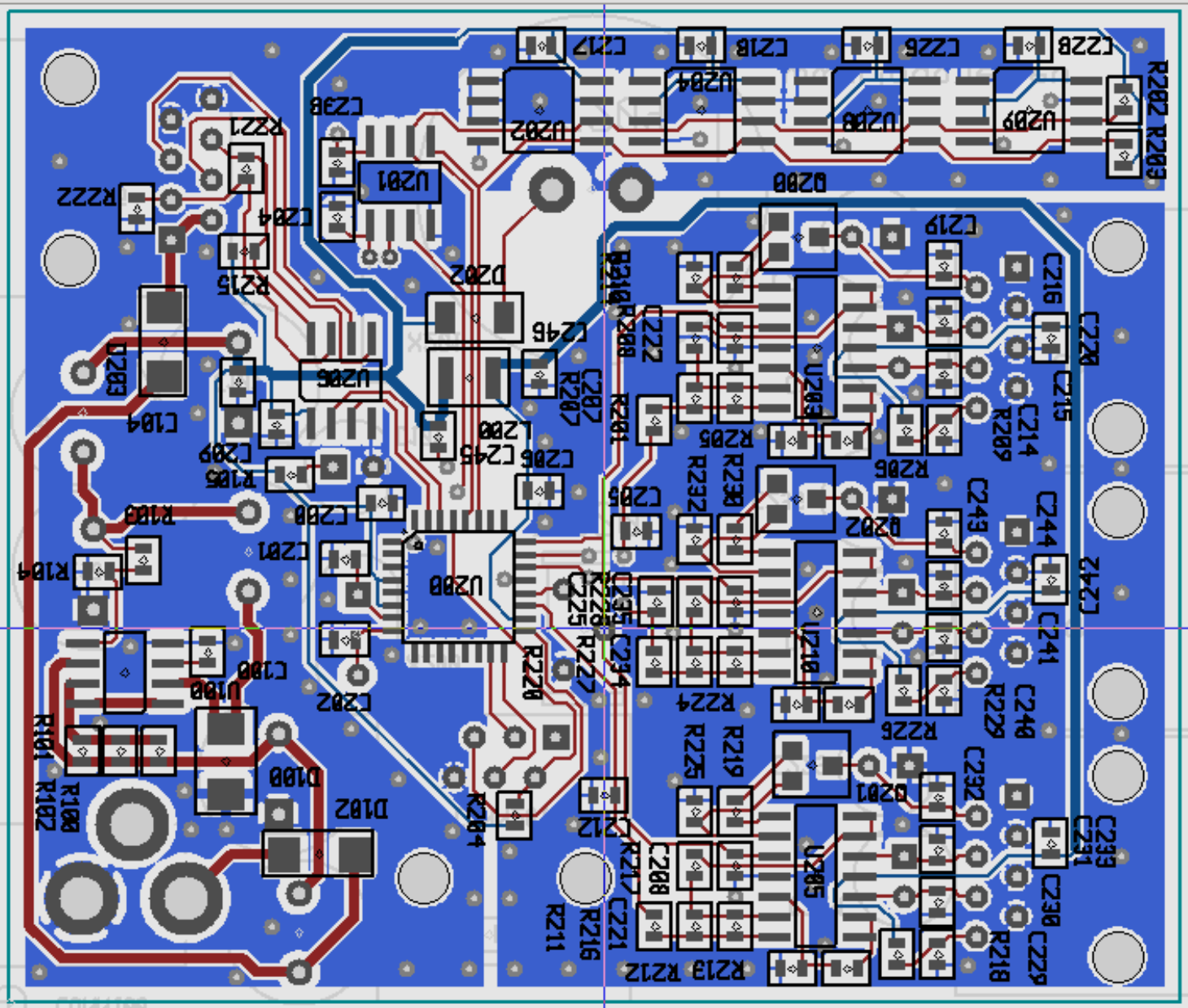
Vcc-sldr
component
GND-comp
Vcc-comp
route
pcb_outline
silk
rat lines
pins/pads
vias
far side
solder mask

VIA LINE ARC
TEXT RECT POLY
BUF DEL ROT
INS THRM SEL
LOCK

Route Style
Signal
Power
Fat
HiPOWER



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chitlesh - Dolphin | PCB: temp_collector | 15:35:22 Fri, 8 May

OVERVIEW : FEDORA'S HIGH END HARDWARE DESIGN PLATFORM

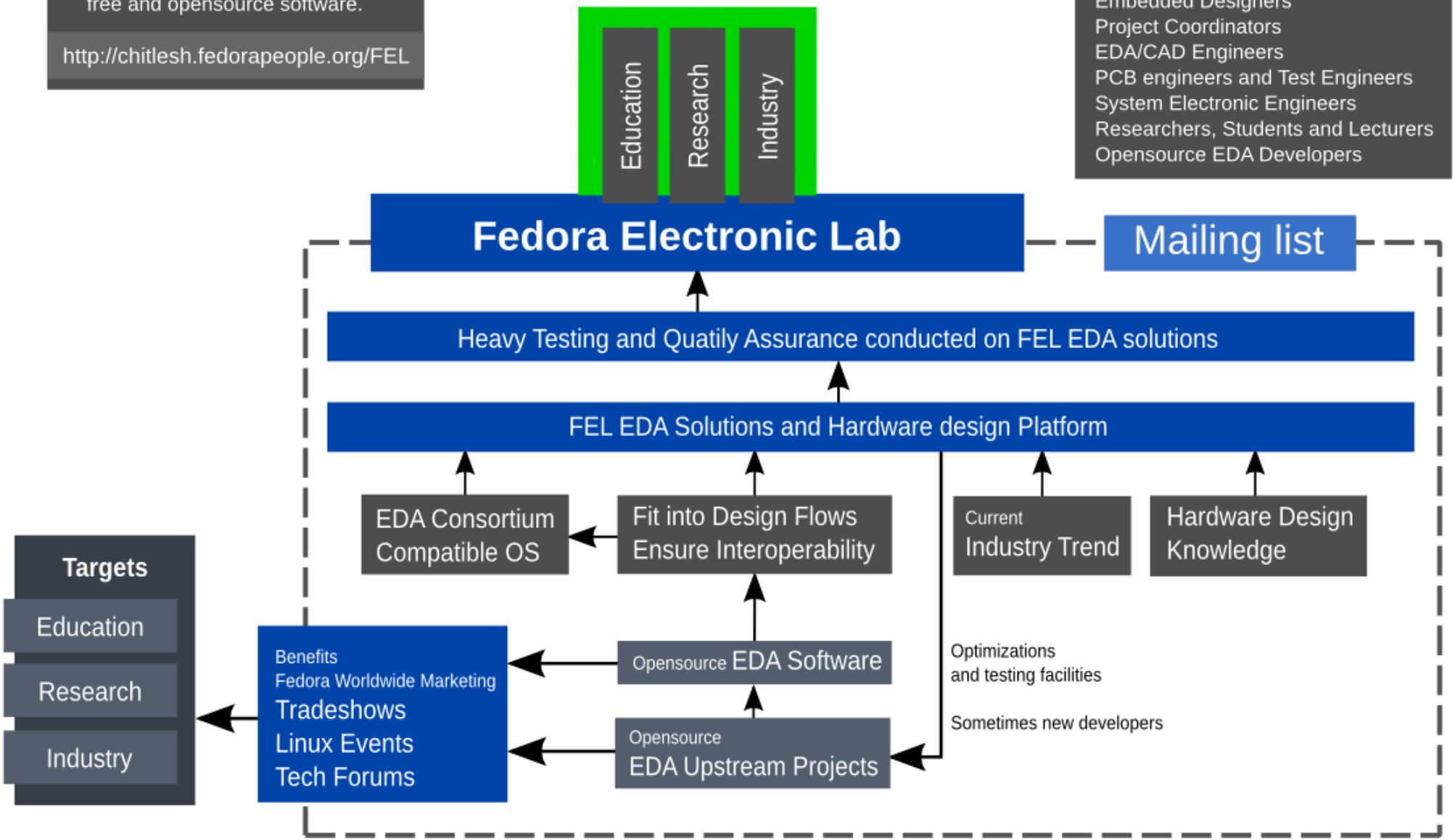
Fedora Electronic Lab

Fedora Electronic Lab improves hardware design experience with free and opensource software.

http://chitlesh.fedorapeople.org/FEL

Benefits

Analog/Digital/Mixed Designers
Verification solutions
Embedded Designers
Project Coordinators
EDA/CAD Engineers
PCB engineers and Test Engineers
System Electronic Engineers
Researchers, Students and Lecturers
Opensource EDA Developers



FEL Development Methodology

The reason why FEL is so unique

All languages win

Bottom Up and Top down research Abstraction

Current Industry Trend

Do not package one's favourite tools only

Think Methodology and Design Flow

Development Time during One cycle

Upstream Talks
Building EDA community

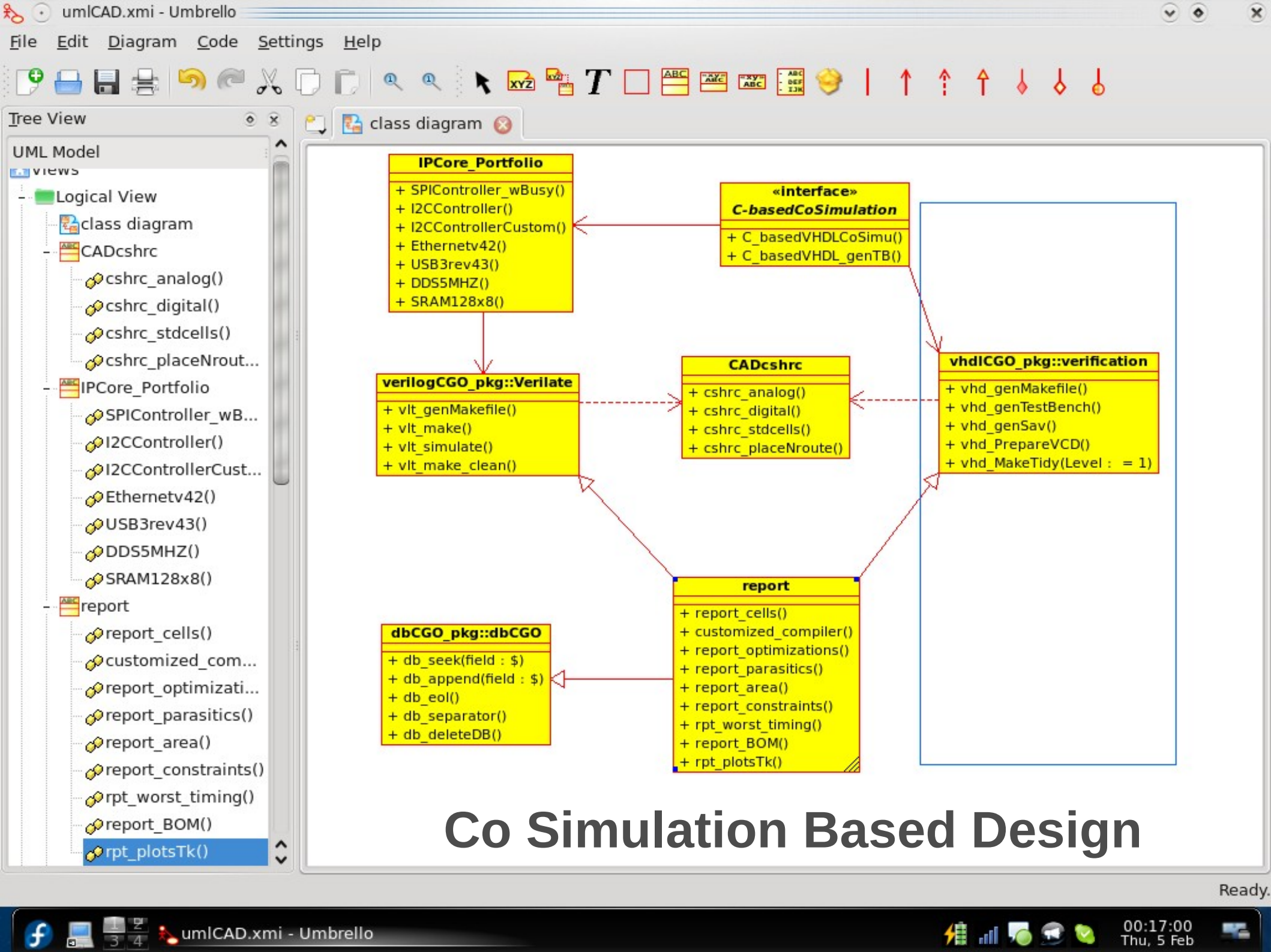
Fixing the World
Marketing

Feedbacks
And wishes

Industry Trend
Market Research
Meet the Outside World

Fedora Packaging
And updates

FEL LiveDVD


umlCAD.xmi - Umbrello
File Edit Diagram Code Settings Help
Tree View
UML Model
Logical View
class diagram
CADcshrc
cshrc_analog()
cshrc_digital()
cshrc_stdcells()
cshrc_placeNrout...
IPCore_Portfolio
SPIController_wB...
I2CController()
I2CControllerCust...
Ethernetv42()
USB3rev43()
DDS5MHZ()
SRAM128x8()
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report_cells()
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report_optimizati...
report_parasitics()
report_area()
report_constraints()
rpt_worst_timing()
report_BOM()
rpt_plotsTk()
class diagram
IPCore_Portfolio
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+ I2CController()
+ I2CControllerCustom()
+ Ethernetv42()
+ USB3rev43()
+ DDS5MHZ()
+ SRAM128x8()
«interface»
C-basedCoSimulation
+ C_basedVHDLCoSimu()
+ C_basedVHDL_genTB()
verilogCGO_pkg::Verilate
+ vlt_genMakefile()
+ vlt_make()
+ vlt_simulate()
+ vlt_make_clean()
CADcshrc
+ cshrc_analog()
+ cshrc_digital()
+ cshrc_stdcells()
+ cshrc_placeNroute()
vhdlCGO_pkg::verification
+ vhd_genMakefile()
+ vhd_genTestBench()
+ vhd_genSav()
+ vhd_PrepareVCD()
+ vhd_MakeTidy(Level : = 1)
report
+ report_cells()
+ customized_compiler()
+ report_optimizations()
+ report_parasitics()
+ report_area()
+ report_constraints()
+ rpt_worst_timing()
+ report_BOM()
+ rpt_plotsTk()
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+ db_seek(field : $)
+ db_append(field : $)
+ db_eol()
+ db_separator()
+ db_deleteDB()
Co Simulation Based Design
Ready.
umlCAD.xmi - Umbrello
00:17:00
Thu, 5 Feb

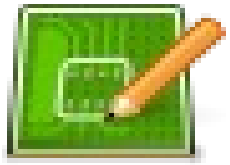
Who are using FEL ?

Universities around the world
- US, France, India, Mexico, Brazil, Italy

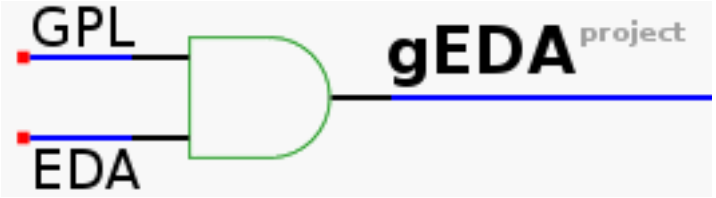
Small companies & consulting companies

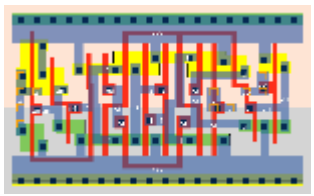
Linux For You magazine
Published twice (Jan 08, Jan 09)

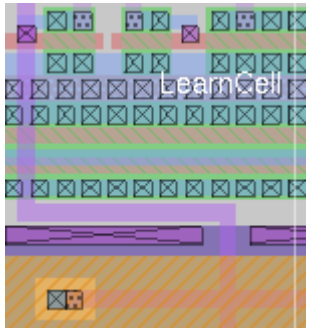
Basic opensource EDA tools
Sun Microsystems, IBM, ST Microelectronics, Analog Devices, On Semi conductors



FEL-12 Constantine







Peer Review possibilities

Hoping gEDA/gaf 1.6

Ktechlab new release

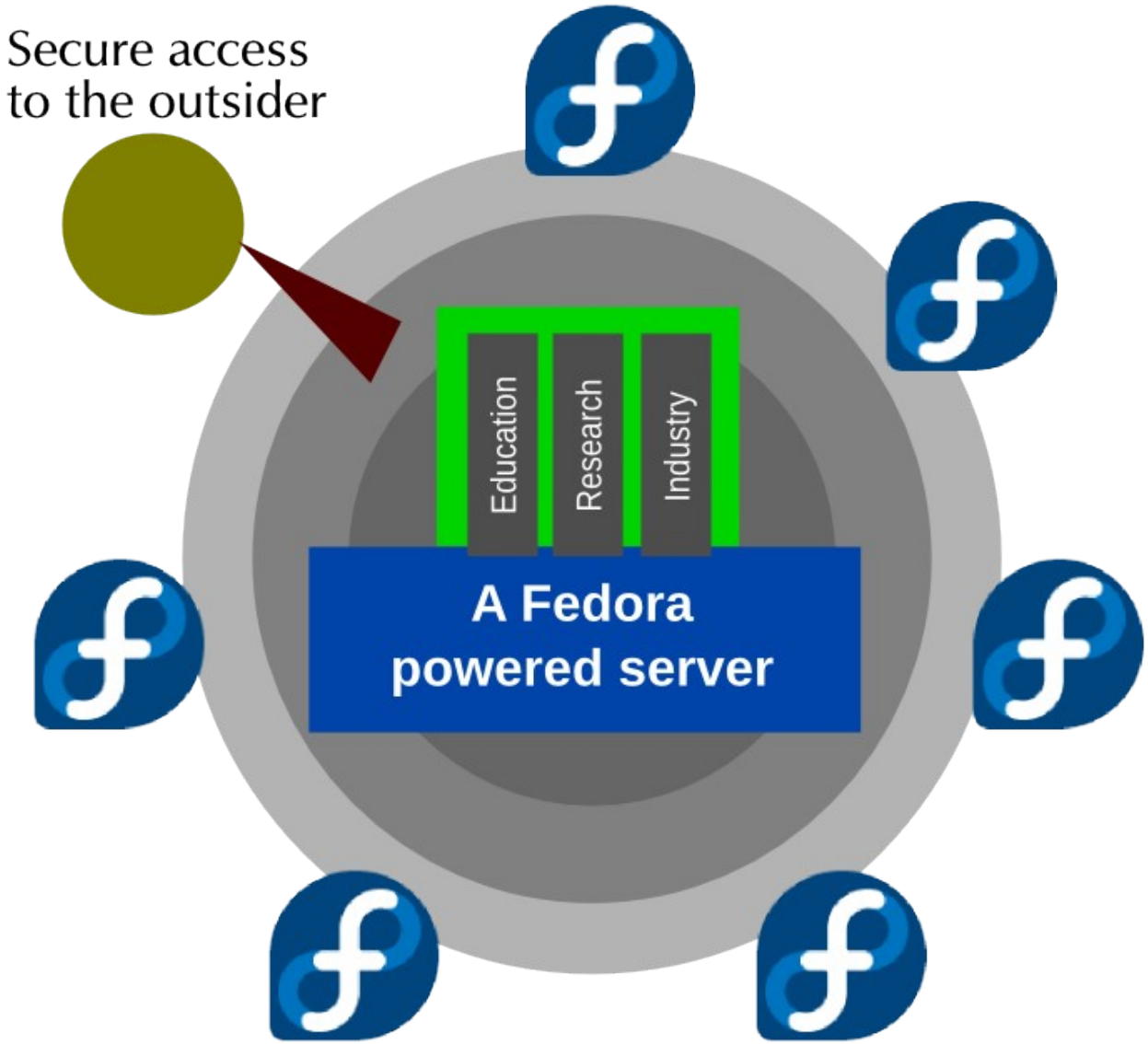
C-based synthesis tool verilator

Centralized location for documentation

OVM/SystemC dropped

Fedora : Collaborative hardware development

Fedora Electronic Lab



http://chitlesh.fedorapeople.org/FEL

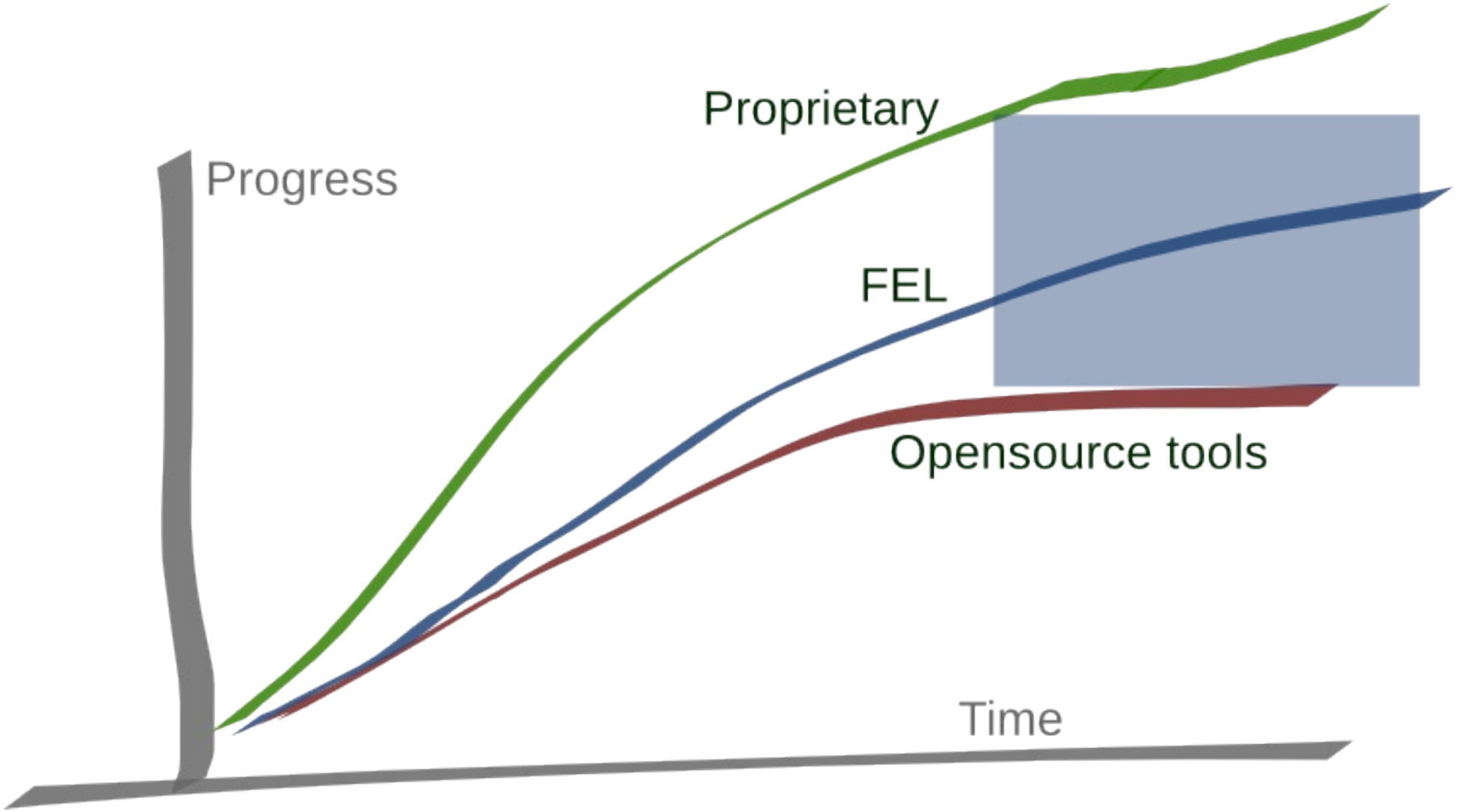
Deployment of a simple Code Review Solution for
- digital IC design
- FPGA design
- embedded design

A Fedora powered server hosting a wiki, web-based version control, progress tracking feature, ticketing service and peer review feature.

Fedora desktops with electronic design and simulation tools coupled with Fedora Eclipse and its plugins.

From Fedora Eclipse, easy and simple HDL code management along with code review via a browser.

FEL User and Developer benefits



Applications Places System fedora 00:24 Sun Jun 28, 02:15:37

Google Reader (1000+) - Mozilla Firefox 3.5 Beta 4

https://www.google.com/reader/view/#overview-page

Productive marketing

Google Reader (1000+)

Mail Calendar Documents Photos **Reader** Sites Web more ▾ chitlesh@gmail.com | Settings | My Account | Help | Sign out

Google reader All items Search

Add a subscription

All items (1000+)

Friends' shared items

Subscriptions

- Adventures in ASIC Di... (1)
- Design And Reuse - In... (15)
- Doug's MATLAB Video T... (1)
- F1technical.net . For... (8)
- File Exchange Pick of... (1)
- Cadence Community (33)
- Fedora People (113)
- Practical Chip Design (2)
- FPGA Blog (3)
- JB's Circuit (1)
- John's Semi-Blog (2)
- MATLAB Central - File... (1)
- my thoughts about VLS... (1)
- Planet Grep (29)
- System-Level Design (8)
- Programmable Logic De... (37)
- Seth on Simulink (1)
- The Digital Electroni... (1)
- The TeX community agg... (1)
- VLSI Core - Technolog... (1)
- Will Partain's work blog (1)
- Xilinx, Inc (PR) (1)
- BBC Sport | Motorspor... (11)
- Eda (74)
  - EDA Blog (51)
  - EDA Graffiti (20)
  - EDA Thoughts (3)

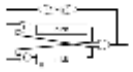
Manage subscriptions »

Home

A look at what's new

Adventures in ASIC Digital Design (1)

Dual Edge Binary Counters + Puzzle I lately came across the need to use a dual edge counter, by this I mean a counter which is counting both on the rising and on the falling edge of the clock. The limitation is that one has to use only normal single edge sensitive flops, the kind you ...



JB's Circuit (1)

Reader Wants Print, not Links *How do the readers of Chip Design - mostly engineers if one believes the polls - prefer to receive editorial content? Print or Online? This question continues to vex both publishers and advertisers/sponsors alike.* *While wrestling with the serious ...

John's Semi-Blog (2)

DAC on Sale Just a quick reminder: DAC 46th Registration Rates go up after June 29, so register today to get the early discount. See you in San Francisco!

Sean Interviews Rajeev Though he's not as colorful as Gerry Hsu, Rajeev Madhavan, CEO of Magma Design Automation, is one of the most interesting and outspoken executives in the EDA industry. Check out Sean Murphy's Interview with Rajeev. Rajeev founded several significant ...

BBC Sport | Motorsport | Formula 1 | UK Edition (11)

Donington given British GP boost Donington's bid to stage next year's British Grand Prix is boosted after final planning permission for its redevelopment programme is approved.

F1 Mole blog F1 is set to play host to Virgin and YouTube next season

Murray Walker Q&A F1 commentary legend answers your British GP questions

VLSI Core - Technology Experts (1000+) (1)

VLSI Conference - Call for papers - January 3-7, 2010 [image: VLSI Design 2010] [image: VLSI Design 2010] [image: VLSI Design 2010] [image: VLSI Design 2010] [image: THEME: Affordable Technology for Emerging Markets] This joint conference is a forum for researchers and designers to present and discuss ...

OpenSemi aggregator (1000+)

Semiconductor News: Buck regulator suits AMD VID interface The MAX17480 fixed-frequency step-down regulator suits the AMD serial VID interface (SVI) CPU. The device features two high-current SMPSs . . . [Source: *Electronic Products* / 06-27]

Semiconductor News: Zigbee IC suits smart energy and HAN apps The EM300 Series ZigBee chip family, consisting of the EM351 and EM357, is suited for smart energy and home ... [Source:

Top Recommendations View all »

National Instruments, Inc.
National Instruments RSS Feed

PowerSource
Technical Editor Margery Conner's PowerSource streams the

Boondoggle B-side
Boondoggle's blog

Recently starred
- Free Online Training: Conformal LEC from *Cadence Community*
- Hiring Begins Again—Slowly from *System-Level Design*

Recently shared
- EDA Installs, the Yum Way? from *Will Partain's work blog*
- Mentor Graphics acquires built-in-self-test specialist from *Fabtech - News*

Recently kept unread
- FPGA software from *EDA Graffiti*
- High performance ARM cores and CAD Reference methodology from *CAD and VLSI*

Recently read
- Red Hat CEO Calls on Oracle to Keep Java Open from *OSNews*
- Vettel gets grandstand at Nurburgring from *F1technical.net . Formula One news*

Tips and tricks

If you find yourself repeatedly visiting a website to check for updates, or if you just stumble across a

Done

Google Reader (1000... fel_fudconBerlin09.od... fel_linuxtag09_f.odp - ...

Research and Development

Read white papers from different companies

Extract information and send to upstream

Write whitepapers for Hardware/IEEE conferences

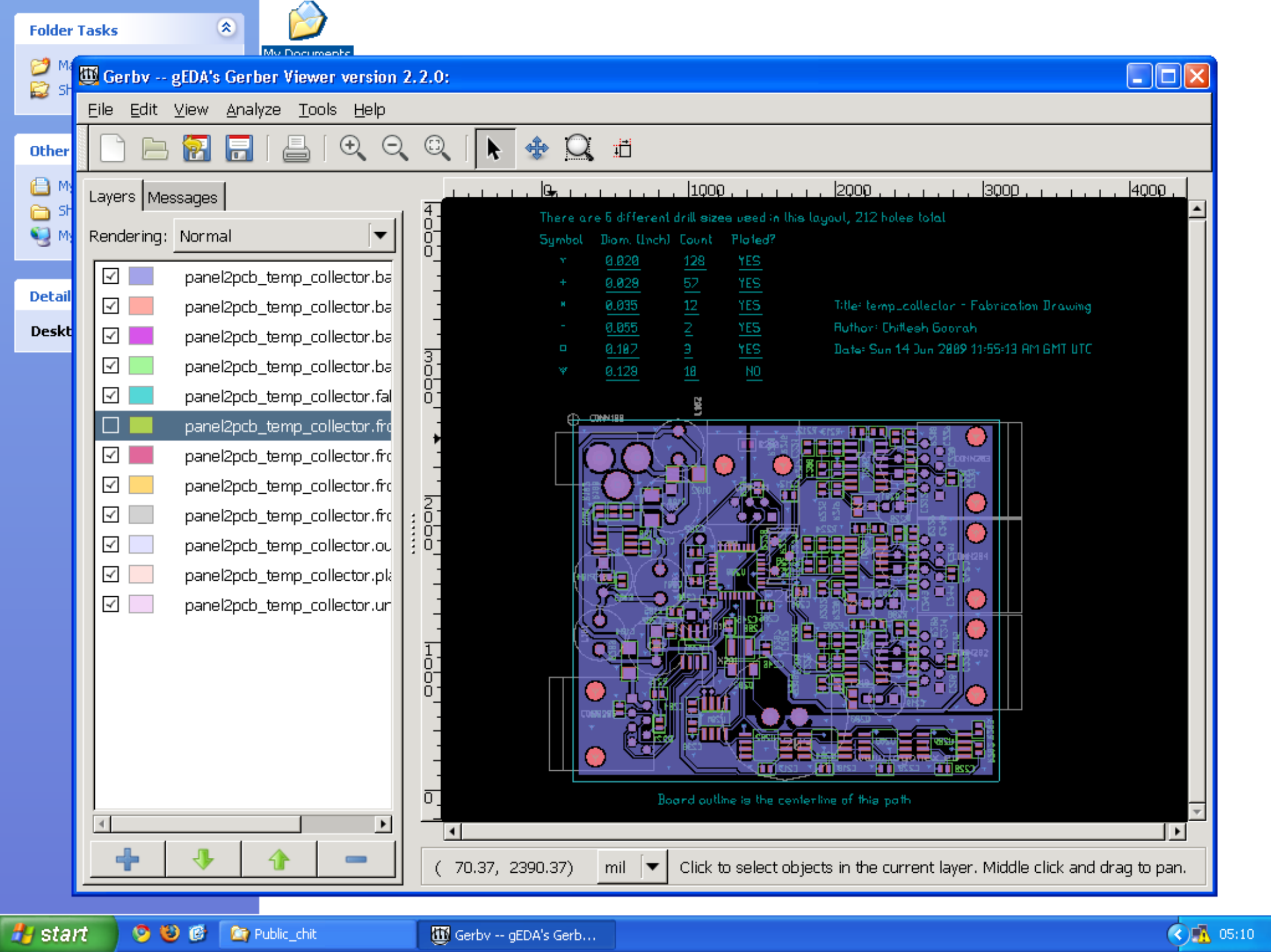
Status Versus EDA Vendors

(Claim == Responsibility)

Collaboration – dataformats, their Opensource software

Using Fedora as a platform for their development

Ensure Productive Marketing for FEL/upstream developers
and NOT Markitecture


Folder Tasks
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Gerbv -- gEDA's Gerber Viewer version 2.2.0:
File Edit View Analyze Tools Help
Layers Messages
Rendering: Normal
panel2pcb_temp_collector.ba
panel2pcb_temp_collector.ba
panel2pcb_temp_collector.ba
panel2pcb_temp_collector.ba
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panel2pcb_temp_collector.ou
panel2pcb_temp_collector.pl
panel2pcb_temp_collector.ur
There are 6 different drill sizes used in this layout, 212 holes total
Symbol Diam. [inch] Count Plated?
r 0.020 128 YES
+ 0.029 57 YES
x 0.035 12 YES
- 0.055 2 YES
□ 0.107 3 YES
▽ 0.129 18 NO
Title: temp_collector - Fabrication Drawing
Author: Chitlesh Goorah
Date: Sun 14 Jun 2009 11:55:13 AM GMT UTC
Board outline is the centerline of this path
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Click to select objects in the current layer. Middle click and drag to pan.
start
Public_chit
Gerbv -- gEDA's Gerb...
05:10

Fedora Infrastructure and services

Simple RPM packaging

Customed KDE kickstart file – LiveCD

fedorahosted
FEL LiveDVD – Spin SIG

Desktop Environment independence
yum groupinstall 'Electronic Lab'
EPEL (users are asking for commercial support)

EDA Industry OS Roadmap

(Updated: September 2007)

Guideline for UltraSPARC Solaris		Sun Website
OS Version	**OS Vendor General Availability**	**Earliest Date for Design Starts**
Solaris 10	January 2005	Now

Guideline for X86 32-bit Windows		Microsoft Website
OS Version	**OS Vendor General Availability**	**Earliest Date for Design Starts**
Windows XP	December 2001	Now
Windows Vista	January 2007	January 2009

Guideline for X86-64 Linux		Redhat & Novell Websites
OS Version	**OS Vendor General Availability**	**Earliest Date for Design Starts**
RHEL 4	February 2005	Now
RHEL 5	March 2007	October 2008
SLES 9	August 2004	Now
SLES 10	July 2006	July 2008

Note

- EDA tool suppliers may exceed the Roadmap baselines.
- Future dates are subject to change.
- For comments or questions about the OS roadmap send an email to OSRoadmap@edac.org

Back to Top

Support Plans of EDA Companies

EDA CONSORTIUM

Long Term goals to achieve

Align FEL along big Vendors in terms of Marketing

Participation in a Standards committee
progress of EDA standards under the IEEE-SA (Standards Association)

Interoperable PDK Libraries

Usage of opensource Industry standard file formats

Strengthen the opensource EDA community

Usage of a common design database

Thank you, Fedora contributors

Questions & Answers


The fedora electronic lab team
fedora-electronic-lab-list@redhat.com