IPCore : Device (v1.00a)

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TABLE I
IPCORE PROJECT SPECIFICATION

Core Specifics		
Supported Family		
Version of core		v1.00a
Budget		
Slices / Logic Elements		
LUTs		
DFFEs		
Block RAMs		
Special Features		
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL/Verilog	
Constraints	UCF/SDC	
Verification	Testbench/PLI	
Inst. Template	Verilog/VHDL Wrapper	
Reference Designs	N/A	
Application Notes	N/A	
Additional Items	N/A	
Perl/Tcl Scripts		
Design Tool Requirements		
Design flow		
Simulation		
Synthesis		
Verification		
Support		
Provided by Chitlesh		

REVISION CHANGELOG

The following table shows the revision history for this document.

Date	Version	ChangeLog
02/03/2008	0.1	Initial draft release

ABSTRACT

This paper entails how

I. FEATURES

II. FUNCTIONAL DESCRIPTION

A. Clocking and Reset

1) Clocking:

2) Reset:

B. Pinouts

TABLE II
DESCRIPTION OF THE I/O SIGNALS IS GIVEN IN THE TABLE:

Signal name	Signal direction	Default Value	Description
*clk	Input	N/A	System clock
i_RstN	Input	N/A	Active low reset

III. DESIGN PARAMETERS

IV. TEST MODE SUPPORT

V. TIMING DIAGRAMS

VI. DESIGN CONSTRAINTS

VII. PERFORMANCE BENCHMARKS

TABLE III
PERFORMANCE AND RESOURCE UTILIZATION BENCHMARK

Budget			F_{max}(MHz)
Slices	DFFE	n-input LUTS	F_{max}

VIII. CHITLESH GOORAH

Fedora's Electronic Lab[1] is a sub-project of the Fedora Project[2].

Chitlesh Goorah holds a master degree in Micro-Nano electronics engineering.

IX. NOTICE OF DISCLAIMER

The information disclosed hereunder is provided AS-IS with no warranty of any kind, express or implied.

REFERENCES

[1] http://chitlesh.fedorapeople.org/FEL
[2] http://www.fedoraproject.org