Release Notes

fedora
ELECTRONIC LAB

Fedora Electronic Lab 12 'Constantine'

Revision   October 3, 2009

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Contents

1 Overview

Revision History

The following table shows the revision history for this document.

Date	Version	ChangeLog	Author
20/07/2009	0.1	Initial draft release	Chitlesh Goorah
10/09/2009	0.1.1	Added PLA, Verilog & 8051 micro-controller related content	Shakthi Kannan
15/09/2009	0.1.2	Added EPEL-5 content & Peer Review methodology	Chitlesh Goorah
29/09/2009	0.1.3	Added geda, picprog and avra content	Chitlesh Goorah
01/10/2009	0.1.4	Updated Toped content	Krustev Svilen
03/10/2009	0.1.5	Draft freezed for release 12	Chitlesh Goorah

Abstract

These release notes present the latest information about Fedora Project's high-end microelectronic design platform : Fedora Electronic Laboratory (FEL)[1] 12. The following section covers new design methodologies, new EDA software, software updates, stability on 64 bit architectures and multiple bug fixes to the existing platform.

Notice

The information provided by this document strictly applies to Fedora Project's product Fedora 12 and the EPEL-5[2] repository. By request of Fedora's user-base some of these features have crawled into the F-10 and F-11 repositories. If any of these items mentioned on this document cannot be reproduced, it should be considered as a bug and be reported to the Fedora Bugzilla[3].

2   Collaborative Code review

One of the many faces of digital hardware design entails tracking many files to be fed to multiple EDA tools. The eventual reports or netlists are carefully analysed and logged as part of the sign-off methodology. Each company tracks these project dependent files under a certain directory structure and under a certain revision controlled system of their choice.

One key feature for the Fedora Electronic Lab 12 release is improving "collaborative hardware development experience" on Fedora. As a test-case scenario, let's imagine 4 persons (from 4 different continents) have encountered each other using a particular social networking medium and want to engage into the development of a FPGA project.
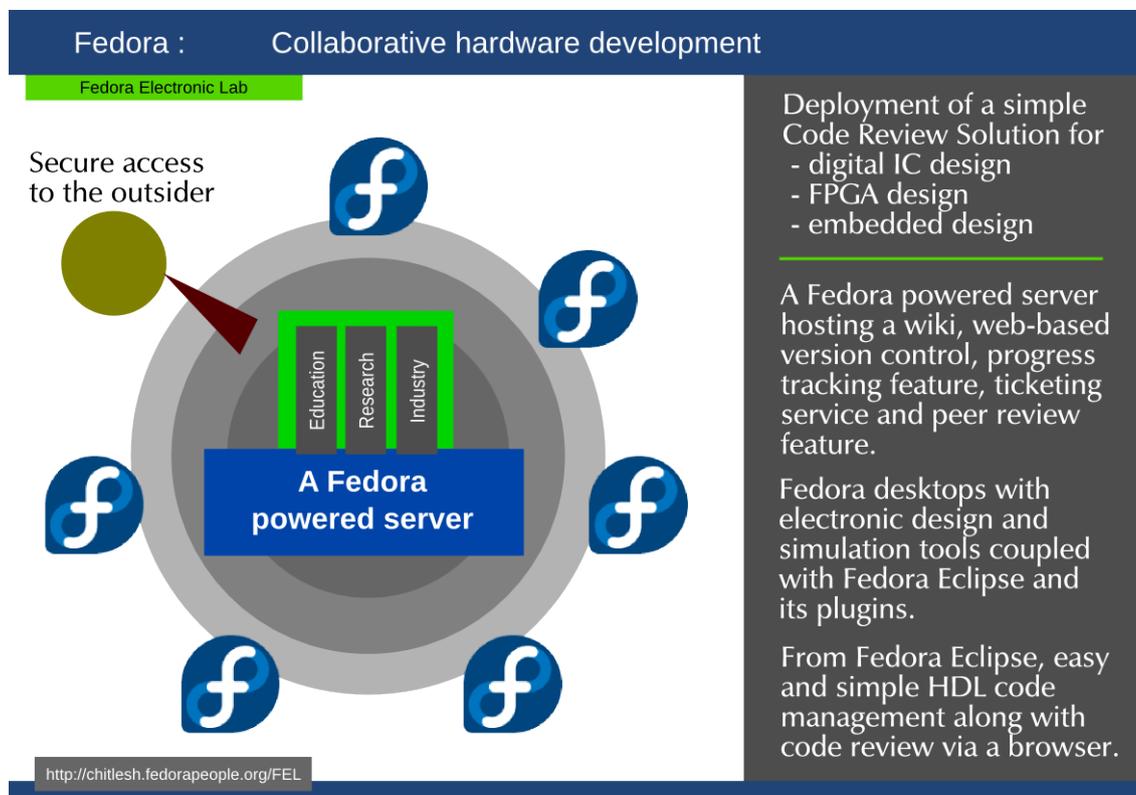
For Fedora 12, we want to ensure that these persons have adequate tools to set up a webserver dedicated for hardware design and help them improve their sign-off and code review methodologies. Hardware code review for small inexperienced companies is often misguided and ends up wasting work hours in unnecessary meetings. Designers often have mixed feelings about code reviews. Sometimes when the code review is outsourced to a third party, source codes are sent in the form of tarballs and tracked as tarballs instead of files,

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which this is no means an efficient way.

We have included an efficient and reliable code review solution into the Fedora collection. This trac-based peerreview solution will also help to create links and seamless references between bugs, tasks, changesets and files. Project coordinators will have a more realistic overview of the on-going project and can track the progress very easy with respect to different milestones and deadlines.

Coupled with Fedora's commitment in Virtualization and SELinux, hardware designers will benefit with a free and robust platform which can easily be deployed.

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3 Eclipse default IDE

With the help and support from Fedora Eclipse team, Eclipse becomes FEL's prime IDE for HDL IP development and documentation. This adoption is to maintain true interoperability between tools offered by different embedded software vendors.

The following plugins provided by default on the Fedora Electronic Lab platform will enhance :

- frontend design
- autogeneration of documentation and maintenance of professional datasheets
- Perl/Tcl scripting (Perl modules which featured since FEL10)
- version controlled projects

Table 1: Eclipse Plugin selected for hardware design.

Package	Description
eclipse-veditor	Helps digital IC designers/FPGA designers develop Verilog/VHDL code on Eclipse.
	Provides a realtime error and warnings notification of typos, missing signals, unnecessary signals etc..
eclipse-eclox	If the vhdl code entails doxygen style comments, a pdf can be autogenerated and used either during internal meetings or sent to the client.
eclipse-texlipse	Since the pdf is generated from latex, the texlipse plugin will provide some additional page layout formatting and easy pdf creation. The pdf creation is now only Ctrl-S, rather than a manual click like one would do on kile. That said, kile was removed from the FEL livedvd.
eclipse-cdt	Provides Embedded C and C++ development tools.
eclipse-dltk-tcl	Tcl scripts can be maintained along side with the HDL code.
eclipse-epic	Perl scripts can be maintained along side with the HDL code.
eclipse-subclipse	Adds Subversion integration to the Eclipse IDE.
eclipse-egit	Adds distributed version controlled GIT integration to the Eclipse IDE

The figure below demonstrates how these Eclipse plugins help to write professional industry datasheets along side the digital/embedded IP.

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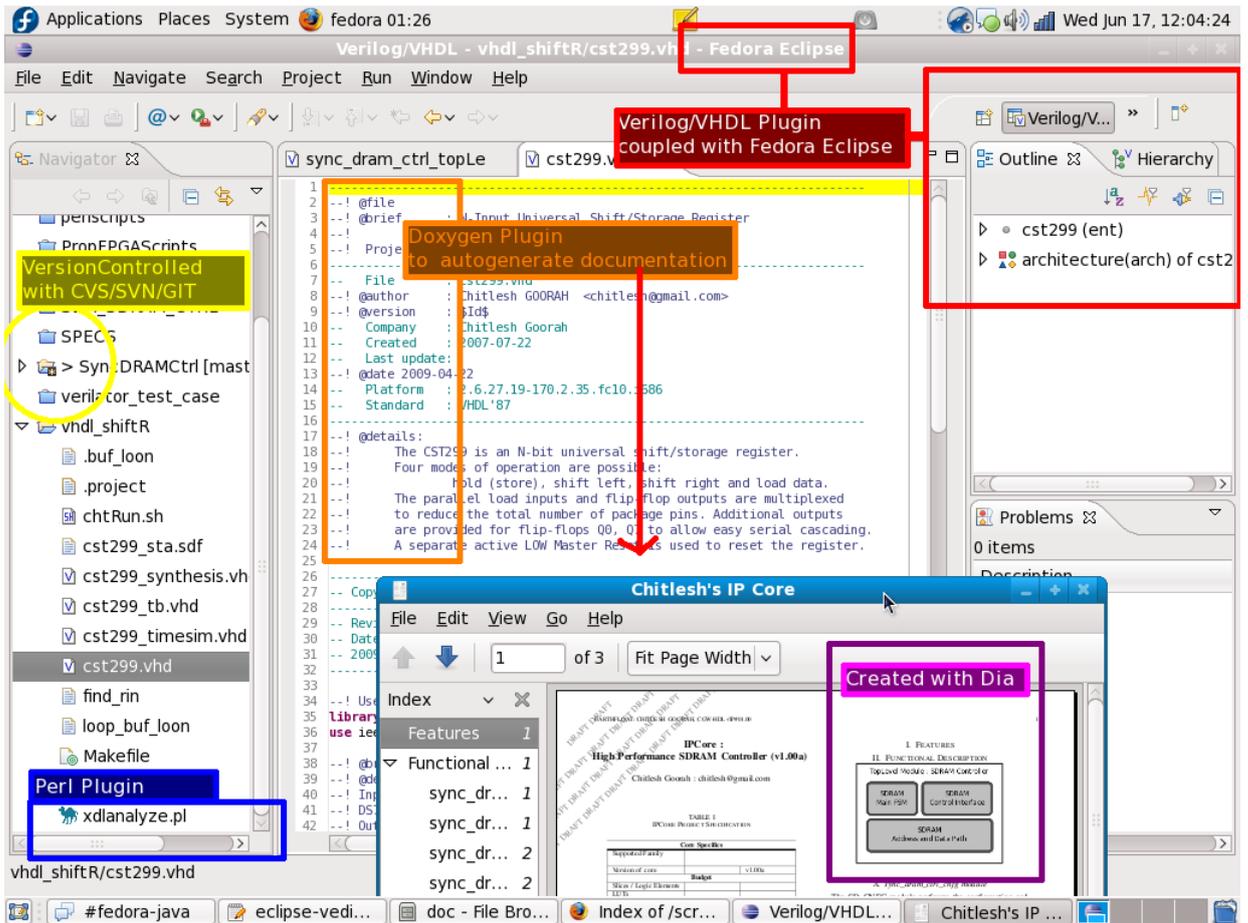
4 Analog ASIC Design

This section describes the changes made on those layout and schematic editors which have been updated.

Toped

Updated to the consolidation release 0.9.5. The Fedora Toped package sets the variable $TPD_GLOBAL to /usr/share/toped by default so that the user could run toped out of the box.

Graham Petley and Krustev Svilen provided 2 TELL files[5] as a demonstration how toped can interact with Pharosc Standard Cells via toped's GDSII and CIF parsers.

Highlights

- New graphic renderer which speeds-up the drawing up-to 3.5 times. Requires openGL version 1.4 and Virtual Buffer Objects. It will be used as a base for future graphical effects.
- The old renderer remains to cover graphic drivers implementing older openGL versions and particularly virtual desktops. F-11 uses openGL 1.3 out of the box, so the the old renderer will be active by default. This is not an issue, because its speed is significantly improved as well.
- The speed is also improved significantly.
- Updates and fixes in the external interfaces. GDSII in particular.
- New utility for conversion of Virtuoso(C) technology files to TELL.
- TDT format updated with new records. Version updated to 0.7.
- Significant improvements in the GDSII conversion speed. Multi gigabyte files are now converted in minutes.
- Further updates on the user interface customization - toolbars.
- Updates in the internal handling of the cell references. In result layer 0 is handled as a normal layer now.
- Provisions on a new Calibre(C) error report parser. Work in progress.
- Many bug fixes.

Caution

Toped releases before 0.94 will not be able to read the new TDT files. The new release should read TDT files independently of the format version.

Magic

Updated to version 8.0.54.

Fedora Magic package has its documentation on a separate package called : magic-doc. The latter includes some examples of scmos and tutorials. Advanced Magic VLSI users would also be interested in reading the documentation again to grasp the fine details entailed in the 8.0 series.

- Features outline vector fonts (courtesy of the freefont project), and aims to clean up a lot of problems associated with labels in Magic.
- All the display, manipulation, and selection routines for both X11 and OpenGL are complete.
- Features some "cifoutput" operators for use with the new "cif paint" command, for manipulating layout using boolean operators.
- Runtime speed has been improved.
- Two additional menus (see figure below) added for grid manipulation and text settings.
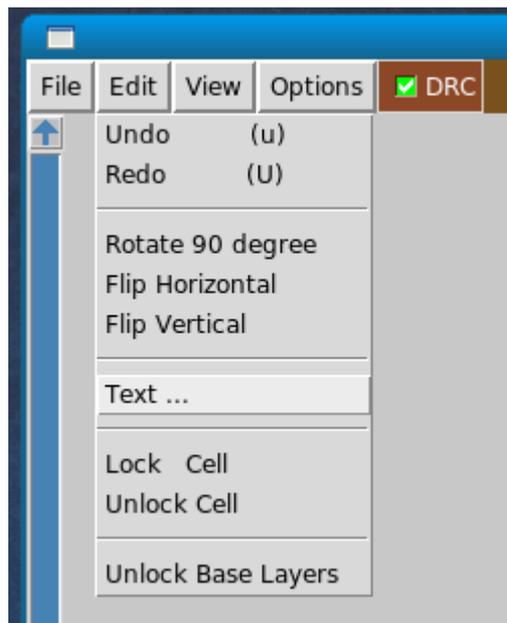
Electric

Updated to version 8.09.

Please note that because most of the electric userbase use third party plugins that due to the licensing incompatibilities wih Fedora, FEL can not add those plugins. That said, Fedora Electronic Lab team understands that releasing a new upstream version would break interoperability with the user's plugins. Hence new versions of electric will once make their way to the updates-testing repository.

Xcircuit

Updated to version 3.6.161.

Highlights

- Supports multiple schematic layout windows.
- A complete overhaul of the key-function binding routines and the function dispatch mechanism was effected.
- The way libraries are handled by making the distinction between library pages and files using the concept of "technology namespaces" has improved. Each object has a name composed of a "technology prefix", a double colon ("::"), and the object's name. Each library file declares a technology name, which is used as the prefix for all objects in that file. The prefixes are used by XCircuit to track which objects came from which file, regardless of the library page onto which they were loaded. Added support for wires connected to symbol pins remain connected while the symbol is moved. It also expands upon the "Attach-to" function, allowing wires to be (semi-) automatically attached to pin labels or symbol pins. The key macro for "attach-to" (key "A") can also be used like the "wire" function (key "w") to start a wire with its start-point attached to a symbol pin or pin label.
- The way info labels for PCB are handled was changed as from version 3.6.66.
- Please read the tutorial to learn the new methods.
- Runtime speed has been improved.
- Fedora's ngspice has been patched to accept calls from Xcircuit TCL interface.

5   Spice Simulation

The figure below demonstrates the interoperability ensured within the Fedora Electronic Lab platform toward spice simulation.
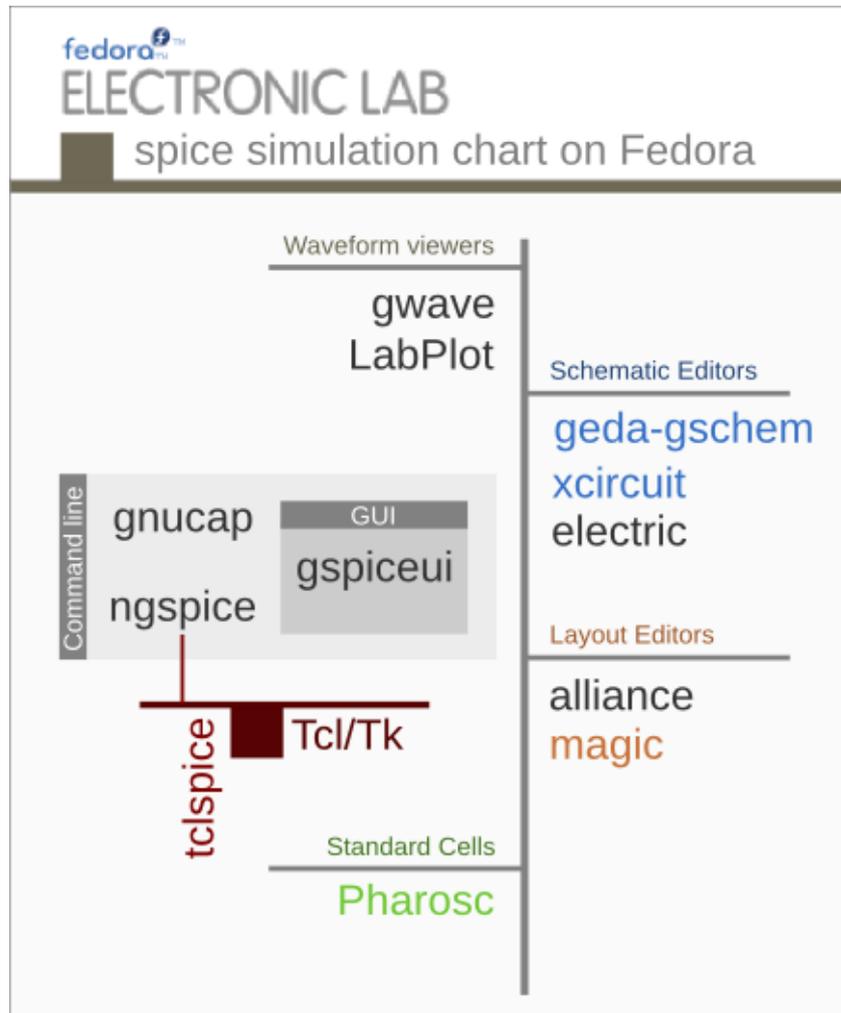
gspiceui

Updated to 0.9.97.

Fedora's GSpiceUI is now compiled under wxGTK 2.8 instead of the old wxGTK 2.6. This improves GSpiceUIi's GUI interface.

Fedora's GSpiceUI includes missing opamp-3.sym to /usr/share/gEDA/sym/misc/ (geda symbols directory).

Added documentations: schematics and spice models

Caution

GSpiceUI is not available on Fedora supported PPC64 architecture as a result of missing gwave for that architecture.

ngspice

Updated to rework 19.

- Memory management: fixed memory leaks (Bug 514484 - A Long Warning Message)
- Integration of espice bugfixes and enhancements
- Bug fixes in plots and cli interface.
- Rework of BSim models, integration of EPFL-EKV model V2.63, ADMS models mextram, hicum0, hicum2.
- Fedora's ngspice has been patched to accept calls from Xcircuit TCL interface.

tclspice

New Package.

Before ngspice-rework-19, Fedora has considered tclspice's stability too fragile. Examples of tclspice can be found via rpm -qd tclspice.

Tclspice provides Fedora users with extended capabilities for mixed-signal design via its TCL backend. Since Fedora is also providing tools for boolean manipulation (explained in the following section), Fedora users have adequate materials to spin his or her own mixed-signal EDA plugin.

6 Embedded Design

avra

New package : version 1.2.3.

Avra is an assembler for Atmel's AVR 8-bit RISC microcontollers. It is mostly compatible with Atmel's own assembler, but provides new features such as better macro support and additional preprocessor directives.

GNUSim8085

New package : version 1.3.5.

GNUSim8085 is a graphical simulator for Intel 8085 microprocessor assembly language. It has some very nice features including a keypad which can be used to write assembly language programs with much ease. It also has stack, memory and port viewers which can be used for debugging the programs.

gsim85

New package : version 0.2.

It is an 8085 microprocessor simulator. It is having very user friendly graphical user interface. It can be used to test 8085 programs before actualy implementing them on target board.

mcu8051ide

New package : version 1.3.

MCU 8051 IDE is integrated development enviroment for microcontrollers based on 8051. Supported programming languages are C and assembly.

It has its own assembler and support for 2 external assemblers. For C language, it uses SDCC compiler.

openocd

New package : version 0.2.0.

The Open On-Chip Debugger (OpenOCD) provides debugging, in-system pro-
gramming and boundary-scan testing for embedded devices. Various different
boards, targets, and interfaces are supported to ease development time.

picprog

New package : version 1.9.0.

Picprog is a simple program for burning programs to various Microchip PIC
microcontrollers via several types of serial port programmers.

gpsim

Updated to version 0.24.0.

Supports for new processors: P10F220, P10F222, P12F675, P12F629, P12F683,
P16F630, P16F676 and P18F4455(No USB support)

*.cod and *.stc files on command line are loaded without -s, -c flag.

Table 2: Closed Sourceforge Bug Reports

RHBZ no.	Title
502665	TMR0 should stop during sleep.
2819395	Multiple CCPs fail in compare mode.
2814950	weak pull-up not disabled for analog pins.
2814946	p18f2455 sigsegv, wrong package size.
2803756	Cannot load a file with "stc" in the filename.
1832222	Port A simulation error in 16f87x.
1629719	"gpsim -p processor file.hex" will work.
2837446	Module library does not load if .so file does not exist.

7 Digital Design

Dinotrace

New package : version 9.4a.

Dinotrace is a waveform viewer which understands Verilog Value Change Dumps, ASCII, and other trace formats.

It allows placing cursors, highlighting signals, searching, printing, and other capabilities superior to many commercial waveform viewers.

Dinotrace is optimized for rapid debugging. With VTRACE, a simulation failure will automatically place cursors where errors occur, add comments visible in the wave form viewer. Four mouse clicks and the errors will be highlighted in the log files, and the values of signals at the error will be seen in the source.

Fedora also ships dinotrace-mode for emacs as emacs-dinotrace-mode.

eqntott

New package : version 9.0.

It converts Boolean logic expressions into a truth table that is useful for preparing input to espresso package for logic minimization, converting logic expressions into simpler forms, and for creating truth tables.

espresso-ab

New package : version 1.0.

Espresso takes as input a two-level representation of a two-valued (or multiple-valued) Boolean function, and produces a minimal equivalent representation. It is a boolean logic minimization tool.

gplcver

New package : version 2.11a.

Cver is a full 1995 IEEE P1364 standard Verilog simulator. It also implements some of the 2001 P1364 standard features. All three PLI interfaces (tf_, acc_, and vpi_) are implemented as defined in the IEEE 2001 P1364 LRM.

GPL Cver is an older version of Cver that is released under the GNU General

Public License. A newer and faster commercial version of Cver is available from Pragmatic C Software Corp.

Verilator

New package : version 3.712.

Verilator is the fastest free Verilog HDL simulator. It compiles synthesizable Verilog, plus some PSL, SystemVerilog and Synthesis assertions into C++ or SystemC code. It is designed for large projects where fast simulation performance is of primary concern, and is especially well suited to create executable models of CPUs for embedded software design teams.

vrq

New package : version 1.0.58.

VRQ is modular verilog parser that supports plugin tools to process verilog. Multiple tools may be invoked in a pipeline fashion within a single execution of vrq. It is a generic front-end parser with support for plugin backend customizable tools.

Alliance

Updated to Snapshot 20090901.

Fedora Alliance CVS devel repository got its 100th patch in August 2009, with respect to stability on 64 architecture and we are happy that upstream has applied all our patches for alliance. We have also built this new release for all Fedora supported testing repositories and EPEL-5 testing repository. There is also a new GUI "xgra" coming with this new release which is a Graph viewer.

We will not replace Alliance VLSI by herb (which was supported to be a fork of alliance) on Fedora. Before F-11's release, herb development was active but died out after F-11 was released. Since Alliance VLSI upstream is active and responsive to our wishes, there is currently no valid reason behind obsoleting alliance in favour of herb.

gnuradio and usrp

Updated to version 3.2.2.

Multiple fixes to ensure compabitility with Python 2.6 and onwards.

iverilog

Updated to snapshot 0.9.20090423.

- VPI bug fix.
- Proper pull ups of user documentation.

tkgate

Updated to snapshot 2.0 Beta 9.

8   Circuit and PCB

fped

New package : snapshot version 5664

fped is an editor that allows the interactive creation of footprints of electronic components. Footprint definitions are stored in a text format that resembles a programming language.

The language is constrained such that anything that can be expressed in the textual definition also has a straightforward equivalent operation that can be performed through the GUI.

gEDA

A lot of effort was sent to prepare the entrance of gEDA 1.6 to stable repositories. That said, geda packages provided by Fedora has undergone review since upstream now ships geda-gaf into one big tarball. Once gEDA 1.6 is released, the existing fedora geda packages will automatically be replaced (transparent to the user) by the new 1.6 release.

With 1.6 release, Fedora users benefit with a metapackage, which allows users to install the complete geda suite with

yum install geda-gaf

Table 3: Closed Sourceforge Bug Reports

RHBZ no.	Title
1758673	Combine source tarballs
2058707	Dangerous button focus in "Save changes" dialog at quit
2430369	Deselecting component doesn't deselect hidden attrib
2449060	Graphic state left inconsistent cancelling from net mode
2460301	Embeded symbol contents different depending on how embedded
2455061	Gnetlist output changed, and tests fail with recent GLib
2655088	autogen.sh doesn't stop on all errors
2823703	Quote problematic pin names in pcbpins
2823755	gnetlist: Compile error with DEBUG=1
2836109	Need to check that groff can create HTML files

libgeda/geda-gschem

- Text rendering is now using native system fonts.
- Image rendering is now using cairo instead of GDK.
- The attribute edit dialog box in gschem now has completion of most common attribute names.
- The multi-attribute edit dialog box in gschem now show unprompted symbol attributes.
- Most menu items in gschem now have icons and properly aligned key bindings.
- Menu accelerator keys are supported as well.
- Assigned shortcuts "vd" and "vl" for changing to the dark or light color schemes in gschem.
- Changed the focus to the "save" button in the close confirmation dialog box in gschem (and gattrib).
- Cleaned up the slot dialog box in gschem.
- Changed the grip size rendering in gschem to be reasonably sized when zooming a lot.
- Introduced a a new attribute searching API.
- The Spanish translation has been updated.
- Lots of code, infrastructure, and doxygen documentation cleanup and refactoring.

geda-gnetlist

- gschem2pcb and PCBboard gnetlist backends have been removed; all users should continue using gsch2pcb.
- gnetlist does not recommend the drc2 backend every time it runs; the drc2 backend is only useful in certain circumstances.

geda-gsymcheck

- Consistent style doxygen documentation is now generated.
- Fixed the test suite for out-of-source directory builds.
- Fixed a whole bunch of minor bugs in the test suite.

geda-gattrib

- Many doxygen comment improvements made to gattrib.
- The unimplemented "File -> Open" menu option has been removed.
- Added –disable-gattrib command line flag to ./configure to disable the building of gattrib when using gtk+ 2.17.x

geda-utils

- gsch2pcb checks for and rejects non-footprint PCB files.
- tragesym now accepts empty attributes in the src file.

geda-symbols

- All of the old vector font definitions have been removed.
- Recursive make is used significantly less when inside the symbols directory.

gerbv

Updated to version 2.3.0.

draw.c and draw-gdk.c functions are used in gerbv.c which is part of libgerbv. Since there is -no-undefined, we require libgerbv to be fully self contained so move draw.c and draw-gdk.c over to libgerbv.

Applied patch to src/draw-gdk.c to fix small error in FAST mode arc rendering.

Fedora Gerbv includes a fix to prevent segmentation fault when modifying non existent layer.

Kicad

Updated to snapshot revision 1863.

Fedora's Kicad will follow OpenMoko's development needs. That said, it will require Fedora's Kicad be pulled from trunk. But, stability of kicad will be ensured. One of the goals of FEL is not to just talk how opensource software is good, but also to support opensource hardware development.

9   Perl Scripts for Hardware design

perl-SystemPerl

New Package : version 1.331.

SystemPerl is a version of the SystemC language. It is designed to expand text so that needless repetition in the language is minimized. By using sp_preproc, SystemPerl files can be expanded into C++ files at compile time, or expanded in place to make them valid stand-alone SystemC files.

perl-Verilog-Perl

Updated to version 3.123.

- Improved warning when "do" used as identifier.
- Fixed escaped preprocessor identifiers, bug106.
- Fixed Perl 5.8.8 compile error, rt48226.
- Fixed Perl 5.8.0 compile error with callbackgen.

Caution

perl-Verilog-Perl obsoletes perl-Verilog. Fedora users are advised to tune their home-made Perl scripts accordingly.

10   EPEL-5 Repository

The following packages of the FEL collection are already available under the EPEL-5 repository. As far as I have tested with commercial EDA tools, the EPEL-5 maintains compatibility and provides a common ground for those who want to have both opensource EDA tools and proprietary EDA tools (assuming they know how to get those proprietary software).

Please note that FEL packages will not undergo constant updates under EPEL-5 compared to the Fedora repositories. Hence you will mostly find the support of newer standards, features and new interoperability solutions available first on Fedora, then they might hit EPEL-5 if proper testing has been carried out.

EPEL-5 repository maintains compability with CentOS-5 and RHEL-5. Please read the Fedora wiki page[2] for installation procedures.

Fedora Electronic Lab collection can be installed (if the node is configured for EPEL-5 branch) with

yum groupinstall 'Electronic Lab'

1. alliance - VLSI EDA System
2. dinotrace - Waveform viewer for electronics
3. dfu-programmer - A Device Firmware Update based USB programmer for Atmel chips
4. electric - Sophisticated Java based VLSI CAD System
5. emacs-dinotrace - Elisp source files for dinotrace under GNU Emacs
6. emacs-verilog-mode - Verilog mode for Emacs
7. emacs-vregs-mode - Elisp source files for systemc-vregs under Emacs
8. eqntott - Generates truth tables from Boolean equations
9. espresso-ab - A boolean minimization tool
10. freehdl - GPLed free VHDL
11. geda-docs - Documentation for gEDA
12. geda-examples - Circuit examples for gEDA
13. geda-gattrib - Attribute editor for gEDA
14. geda-gnetlist - Netlister for the gEDA project
15. geda-gschem - Electronics schematics editor
16. geda-gsymcheck - Symbol checker for electronics schematics editor
17. geda-symbols - Electronic symbols for gEDA
18. geda-utils - Several utilities for the gEDA project
19. gerbv - Gerber file viewer from the gEDA toolkit
20. gnucap - The Gnu Circuit Analysis Package
21. gplcver - An interpreted Verilog HDL simulator
22. gtkwave - Waveform Viewer
23. irsim - Switch-level simulator used even for VLSI
24. iverilog - Icarus Verilog is a verilog compiler and simulator

25. linsmith - A Smith charting program
26. magic - A very capable VLSI layout tool
27. mcu8051ide - IDE for MCS-51 based microcontrollers
28. netgen - LVS netlist comparison tool for VLSI
29. ngspice - A mixed level/signal circuit simulator
30. octave-forge - Contributed functions for octave
31. pcb - An interactive printed circuit board editor
32. perl-Hardware-Verilog-Parser - Grammar for parsing Verilog code using perl
33. perl-Hardware-Vhdl-Parser - Grammar for parsing VHDL code using perl
34. perl-ModelSim-List - Analyse the 'list' output of the ModelSim simulator
35. perl-Perlilog - Verilog environment and IP core handling in Perl
36. perl-SystemC-Vregs - Utility routines used by vregs
37. perl-Verilog - Verilog parsing routines
38. perl-Verilog-CodeGen - Verilog code generator
39. perl-Verilog-Readmem - Parse Verilog $readmemh or $readmemb files
40. qemu - QEMU is a FAST! processor emulator
41. qucs - Circuit simulator
42. tkcvs - TkCVS and TkDiff
43. toped - VLSI IC Layout Editor
44. trac-peerreview-plugin - Framework for realtime code review within Trac
45. tkgate - An event driven digital circuit simulator
46. vhd2vl - VHDL to Verilog translator
47. vym - View your mind
48. xcircuit - Electronic circuit schematic drawing program

11   Submenu support on electronics-menu
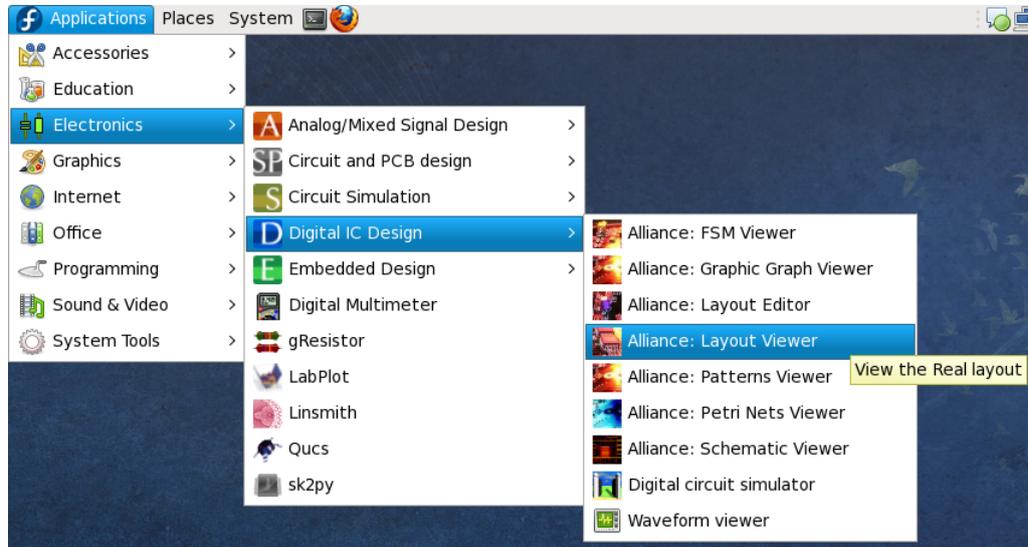
The above screenshot describes these submenus which will be default on F-12. There are currently five standard design flows for the average user:

- Analog/Mixed Signal Design
  Any EDA software with respect to analog IC design, e.g magic, xcircuit, toped, electric,. . .
- Circuit and PCB Design
  EDA software to create schematics and PCB layouts, e.g geda-gaf, PCB, kicad,. . .
- Circuit Simulation
  Spice simulations and waveform viewers.
- Digital IC Design
  Frontend and Backend digital design tools and waveform viewers.
- Embedded Design
  8051 and 8085 microprocessor simulators and PIC simulators and programmers.

12   Bugzilla Reports and Closed Tickets

Table 4: Closed Bugzilla Reports

RHBZ no.	Package	Title
389281	pharosc	symlinks and packaging
488046	gnuradio	fails with python 2.6 and onwards
511400	perl-SystemPerl	New: Header Include Bug in SystemPerl
511682	iverilog	FTBFS iverilog-0.9.20090423-4..fc11
511695	ngspice	FTBFS ngspice-18-2.fc11
512076	gspiceui	Build with wxGTK-devel not compat-wxGTK26-devel
513903	gwave	F9+: gwave fails to display data and crashes using: File->Read File...
514484	ngspice	A Long Warning Message
515407	kicad	Please update Kicad to the new release
517482	octave	crashes on "clear all"
518916	kicad	Incorrect multilib path

Table 5: Closed Tickets on Fedora Hosted

Tickets no.	Package
6	SystemC and Fedora 10
8	Design/Code Review
12	package openocd
13	perl-Verilog-CodeGen's Tk based GUI should be revisited
14	Component libraries
15	FEL with source + build packages
18	package gplcver
19	package a 8051 ide (spec included) embedded design
21	package veditor for eclipse
22	package of GNUSim8085 which is a nice 8085 simulator
23	Package qtdmm
24	package espresso - it's said that even cadence based their tools from it
26	package perl(IEEE.std_logic_1164.all)
27	wishbone builder (spec draft included)
33	need help for Kicad
35	alliance 64 stability
36	Groupinstall not listed in "Add/Remove Software"
42	to package : Verilog Tool Framework
47	gerbv-2.3.0-1 png failed to open
48	(tracker) verilog-mode update on Fedora rawhide

About Fedora Electronic Lab

Fedora's Electronic Lab[1] is a sub-project of the Fedora Project[4] dedicated to support the innovation and development of opensource EDA community. This ambitious sub-project provides a complete electronic laboratory setup with reliable open source design tools in order to keep engineers and researchers in pace with current technological race.

References

[1] `http://chitlesh.fedorapeople.org/FEL`

[2] `https://fedoraproject.org/wiki/EPEL`

[3] `https://bugzilla.redhat.com`

[4] `http://www.fedoraproject.org`

[5] `https://fedorahosted.org/fedora-electronic-lab/browser/testsuite/toped`